Renewed enthusiasm for high-mobility channel development

Mike Cooke reports on presentations on high-mobility III-V and Ge-channel devices at December's International Electron Devices Meeting in San Francisco.

The past year has seen a renewed effort in developing high-mobility channels for high-performance and low-power electronics, at least according to the presentations at the 2012 International Electron Devices Meeting (IEDM) in December. While in previous years the III-V contributions were fairly evenly balanced between narrow-bandgap materials for high mobility and wide-bandgap materials for high power density, the 2012 IEDM seemed dominated by high-mobility reports for logic and radio-frequency devices. In addition to III-V materials, there were important developments in germanium-based devices for p-type (and in some cases n-type) channels.

This is not to say that there were not some important wide-bandgap contributions. For example, HRL Laboratories LLC of Malibu, CA, USA claimed a record cut-off frequency of 500GHz for a nitride semiconductor high-electron-mobility transistor (HEMT) [K. Shinohara et al, session 27.2]. This achievement was based on a process for creating deeply scaled self-aligned-gate gallium nitride (GaN) HEMTs with heavily doped n^+-GaN source/drain (S/D) regions in direct contact with the two-dimensional electron gas (2DEG) channel near the gate. Devices with a gate length of 20nm had an on-resistance of 0.23Ω-mm, maximum drain current of more than 4A/mm, and transconductance of more than 1S/mm over the drain current range of 0.5–3.5A/mm.

Here, however, we will focus on some of the progress presented for producing high-mobility devices on silicon using III-V- and germanium-based semiconductors.

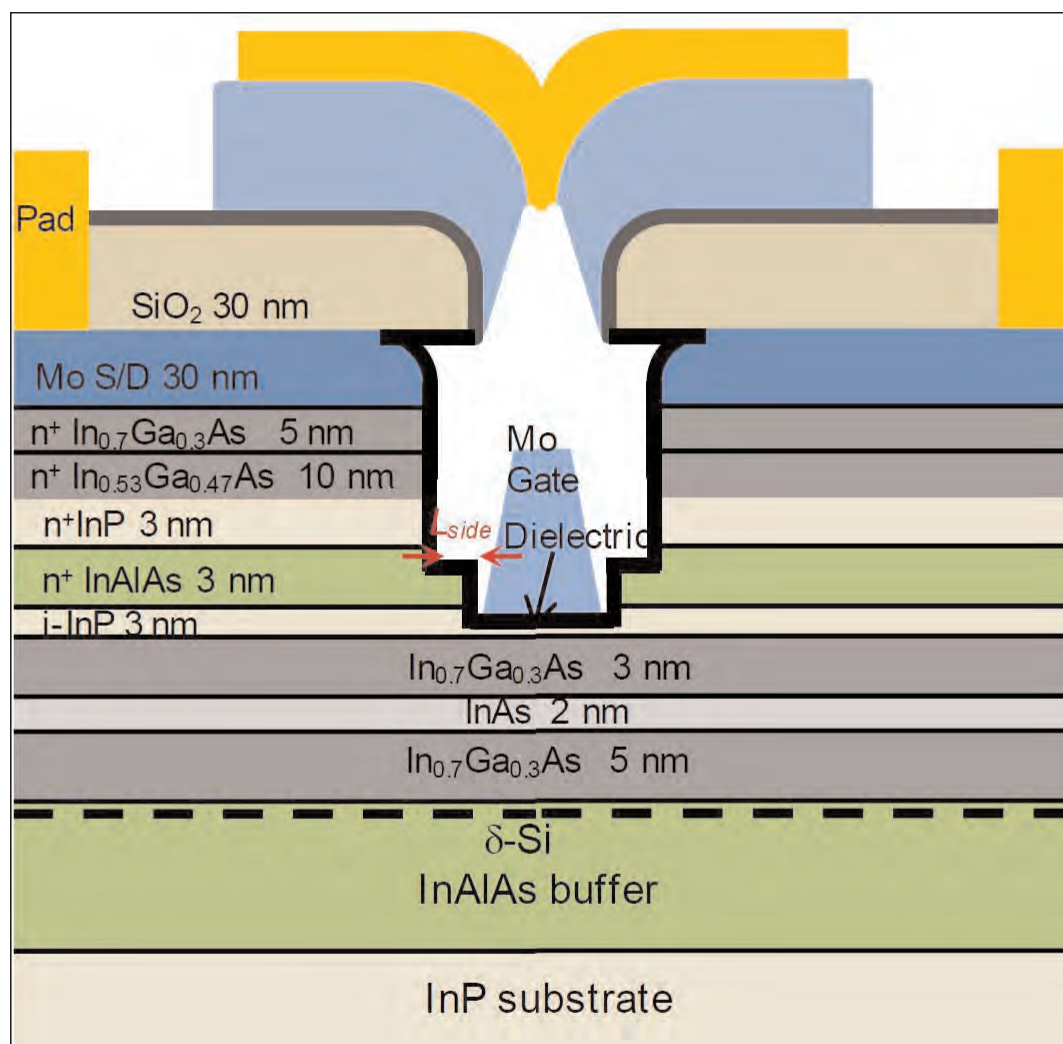

Figure 1. Cross-sectional schematic of MIT's InAs QWMOSFET with ultra-scaled HfO_2/InP composite barrier.

Smallest working III-V transistors

Researchers at Massachusetts Institute of Technology (MIT) claimed the shortest gate for working transistors yet built using III-V channels [J. Lin et al, IEDM, session 32.1]. The metal-oxide-semiconductor field-effect transistors (MOSFETs) were also the first to use self-aligned contacts to reduce the distance between the gate and source-drain regions to 20–30nm. The researchers were keen to reformulate the production processes to more closely resemble those of silicon semiconductor manufacturing. Self-alignment is one such technique.

Matthias Passlack, of Taiwanese semiconductor manufacturer TSMC, commented on the work, led by MIT professor Jésus del Alamo: "He and his team have experimentally proven that indium arsenide channels outperform silicon at small-device dimensions. This pioneering work has stimulated and facilitated the development of CMOS-compatible, III-V-based-technology research and development worldwide."

The MIT research was funded by US Defense Advanced Research Projects Agency (DARPA), Intel and the Semiconductor Research Corporation's Center for Materials, Structures and Devices (FCRP-MSD).

The semiconductor material for the MIT device was produced at Intelliepi using molecular beam epitaxy (MBE) on indium phosphide (InP) substrates (Figure 1). The channel consisted of a quantum well (QW) of indium arsenide (InAs) in indium gallium arsenide (InGaAs) barriers. The upper n^+-InP/n^+-InAlAs/i-InP layers are a 'ledge' designed to lower access resistance between the n^+-InGaAs source-drain contact regions and the QW channel.

Sputtered, low-resistance 5Ω/square molybdenum (Mo) was used for metal contacts. This was covered with silicon dioxide (SiO_2) in a chemical vapor deposition (CVD) process.

The devices were then patterned with electron-beam lithography and mesa isolation and gate formation achieved with reactive-ion etch (RIE) through the SiO_2 and Mo (Figure 2). The RIE damage was repaired using 350°C annealing, the highest temperature used in the entire transistor fabrication process. The gate length was defined by the amount of gate opening, and the researchers believe that this can be scaled to less than 20nm.

Further wet and dry etch steps were used to recess the gate region, leaving about 1nm of the 3nm InP layer above the top InGaAs barrier of the QW. The control of this last etch was achieved through a self-limiting 'digital' technique involving plasma oxidation and dilute sulfuric acid (H_2SO_4).

The gate dielectric consisted of 2nm of hafnium dioxide (HfO_2), applied using atomic layer deposition (ALD). The dielectric was deposited conformally and therefore also provided passivation of the access region between

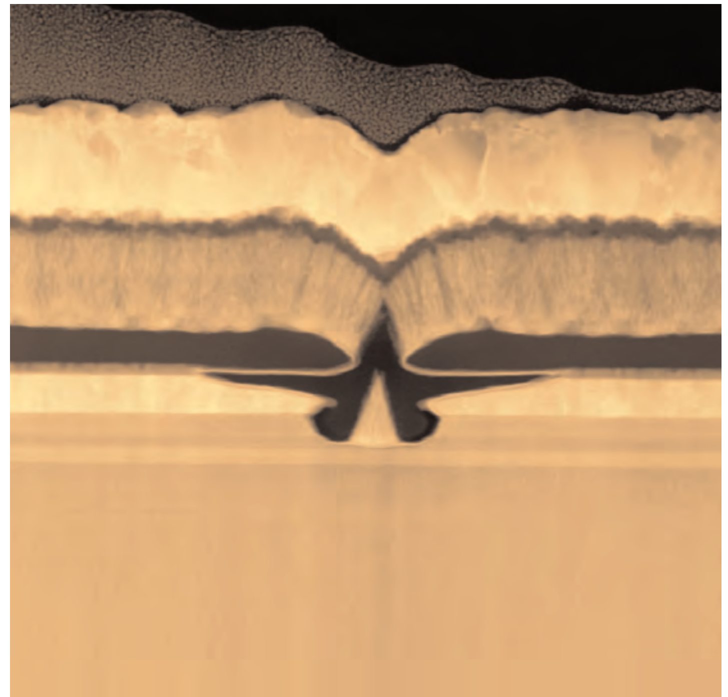

Figure 2. Cross-sectional transmission electron micrograph (TEM) of fabricated MIT transistor. Central inverted V is the gate. Two molybdenum contacts on either side are the transistor's source and drain. The channel is the InGaAs light color layer under the source, drain and gate. Image courtesy of the MIT researchers.

the edges of the gate and the n^+-InGaAs cap. The dielectric had an equivalent oxide thickness (EOT) of 0.4–0.5nm. The total EOT, including the InP barrier, was ~0.8nm. The Mo gate metal was evaporated on and patterned through etching.

The researchers found a source–drain resistance of 445Ω-μm, which they describe as 'relatively high',

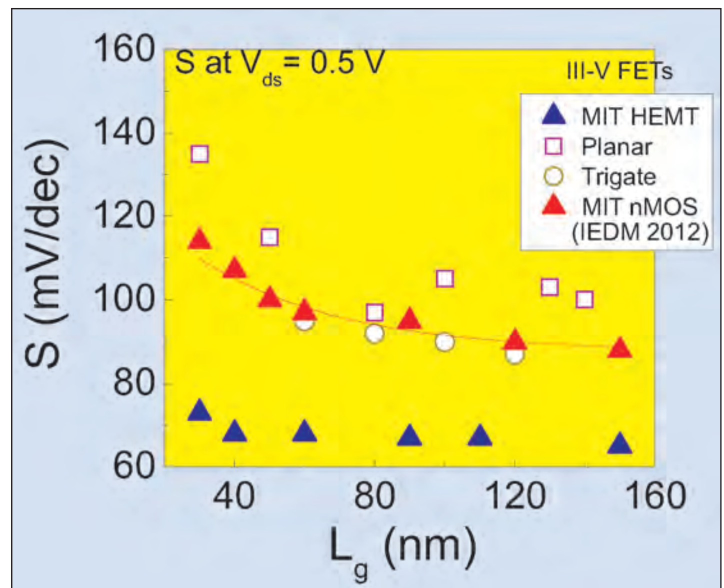

Figure 3. Subthreshold swing (S) vs gate-length at 0.5V for III-V MOSFETs and HEMTs (essentially transistors without gate insulation).

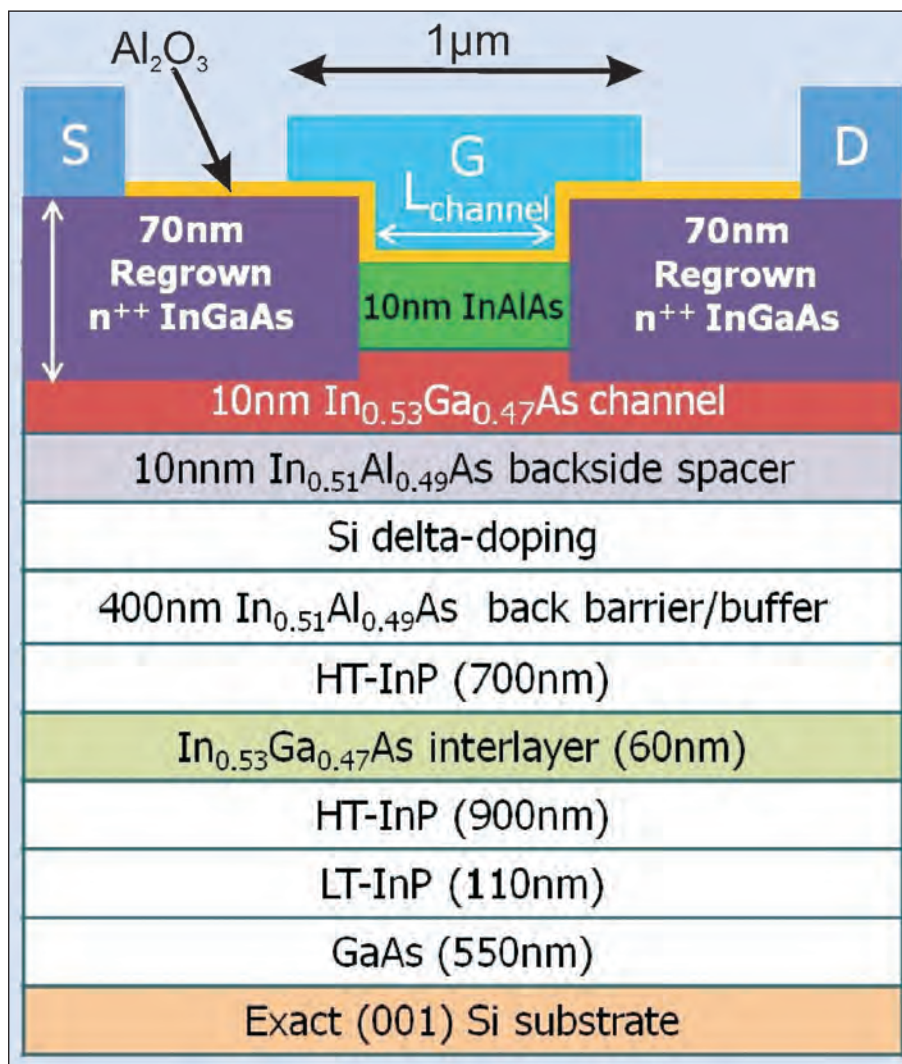

Figure 4. Schematic of HKUST device with nominal layer thicknesses (LT-low temperature, HT-high temperature, figure not drawn to scale).

blaming this on the small uncapped regions of the source–drain stacks (L_{side} in Figure 1). "This can be solved through an improved n^+-InP S/D ledge design," they say.

For a 30nm-gate device, the researchers quote a subthreshold swing of 103mV/dec at 50mV drain bias and 114mV/dec at 0.5V drain bias. The drain-induced barrier lowering was "relatively high" at 236mV/V, related to the heterostructure buffer and not the fabrication process. Despite the HfO_2 insulation being very thin at 2nm, gate leakage was less than 1nA/µm.

With 0.5V drain bias, the peak transconductance was 1420µS/µm (1530µS/µm for 60nm-gate). A 'fully operational' 22nm-gate device had a peak transconductance of 1050µS/µm with 0.5V drain.

Comparing their device with others (Figure 3), the researchers comment: "Our ultra-scaled barrier MOSFETs exhibit a subthreshold swing that is superior to any other planar III-V MOSFET, and that matches the best Tri-gate III-V devices." Also, for sub-60nm-gate transistors, the transconductance performance is "superior to any other planar or Tri-gate III-V MOSFET."

The researchers also produced a variant device with a 15nm InGaAs channel and a composite gate dielectric consisting of 0.4nm aluminium oxide and 2nm HfO_2. A long-gate (300µm) device achieved a subthreshold swing of 69mV/dec, near to the ideal room-temperature value for planar structures of 60mV/dec. This very low value is among the best ever reported for III-V MOSFETs.

A 20µm-gate device had a mobility of 4650cm^2/V-s at a sheet carrier density (N_s) of $4x10^{12}/cm^2$. "This is the one of the highest mobility values at this N_s published in InGaAs MOSFETs to date," the researchers write.

The team plans to next work on improving the electrical performance by reducing the parasitic resistance in these devices. This will enable further shrinking, with the ultimate aim being sub-10nm gate lengths.

Another group at MIT and University of British Columbia Vancouver [W. Chern et al, session 16.5] demonstrated "for the first time asymmetrically strained Ge, high-k/metal gate nanowire (NW) trigate p-MOSFETs with record hole mobility of 1490cm^2/V-s." The researchers add: "This mobility is 2x above on-chip biaxially strained Ge FETs and ~15x above Si universal mobility."

Hong Kong University of Science and Technology has also been developing very short gate-length III-V InGaAs devices (Figure 4) grown directly on silicon using metal-organic chemical vapour deposition (MOCVD) [X. Zhou et al, session 32.5]. The source–drain regions were selectively re-grown with n^+-InGaAs material to reduce access resistance. The contact metals were nickel/germanium/gold/germanium/ nickel/gold. The gate stack consisted of an InAlAs barrier, 6nm of aluminium oxide (Al_2O_3) dielectric and a titanium/platinum/gold gate.

A post-metallization anneal (PMA) was performed in an ALD system (300°C for 5 minutes in nitrogen) to shift the threshold voltage in a positive direction from –1.4V to +0.08V for enhancement-mode/normally-off operation. Another effect of the PMA was enhanced electrostatic control, resulting in the peak transconductance increasing from 1074mS/mm (before PMA) to 1700mS/mm (after). Also, the subthreshold swing with 50mV drain bias was reduced from 172mV/dec to 142mV/dec (after PMA). The on/off ratio (0.5V above/below threshold) was $1.7x10^4$. A maximum drain current was 1327mA/mm at 1.6V gate with 0.5V drain bias.

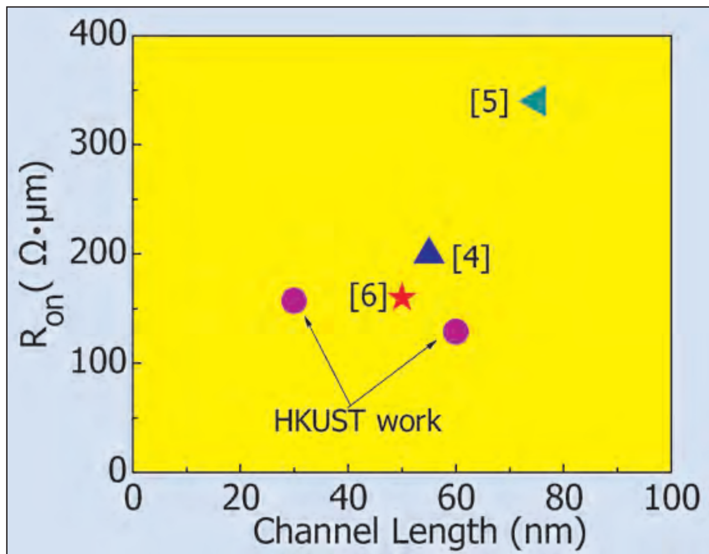

Figure 5. Comparison of HKUST R_{on} with state-of-the-art InGaAs MOSFETs.

Compared with other groups (Figure 5), the HKUST device had the lowest on-resistance, at 157Ω-μm. The researchers comment: "We attribute the impressive R_{on} to the high-quality S/D re-growth with high doping level." The same group has recently reported even lower on-resistance in a similar 30nm-gate device with a record 133Ω-μm [Xiuju Zhou et al, IEEE Electron Device Letters, vol33, p1384, 2012].

A longer 60nm channel achieved a lower subthreshold swing of 101mV/dec with 50mV drain bias.

The researchers suggest that one effect of the PMA is to repair damage from the electron-beam evaporation process. For example, the titanium gate layer becomes smoother and more dense after PMA. Energy-dispersive x-ray spectroscopic analysis also showed the presence of oxygen in the metal layers before PMA but not after.

Setting up for 4D electronics

Purdue and Harvard universities presented stacked InGaAs nanowire (NW) transistors with increased drive current and maximum transconductance [J.J. Gu, X.W. Wang et al, IEDM 2012, session 23.7]. Since the nanowire transistors already have 'three dimensional' (3D) wrap-around gates, the extension into stacking has been labeled '4D electronics' (Figure 6).

The researchers have built on their previous work with transistors produced using indium gallium arsenide (InGaAs) NW channels with the 'gate all-around' (GAA). The Christmas tree-effect is due to the diameter of the nanowires in the upper layers being smaller than in layers below.

The epitaxial layers of III-V material were grown on semi-insulating (SI) InP substrates using molecular beam epitaxy (Figure 7.1). The source/drain regions were defined using a silicon implant at two energies, designed to drive the donor atoms to give a spread of depths uniformly contacting all three nanowire channels

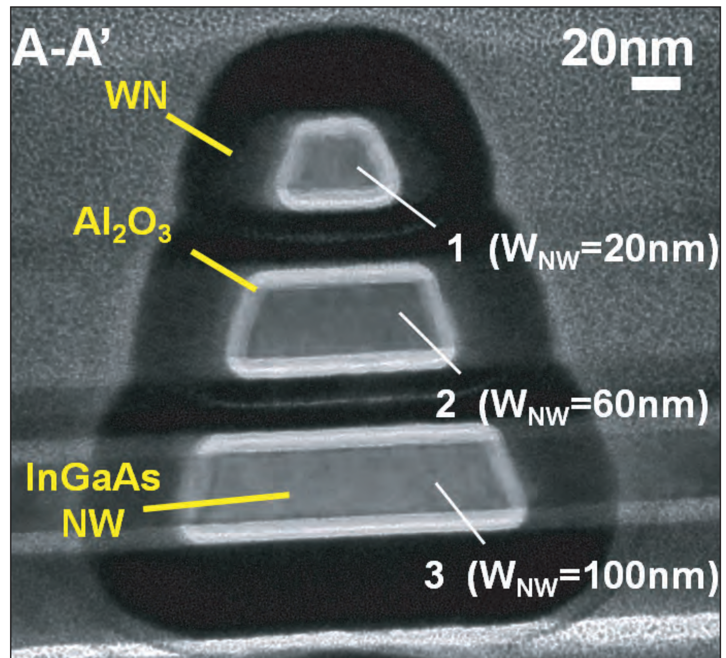

Figure 6. TEM of Purdue/Harvard 4D transistor cross-section.

(see Figure 7.2).

The nanowires were formed by first reactive ion etching of fins in the epitaxial material, using aluminium oxide (Al_2O_3) as a mask (Figures 7.3–5). The Al_2O_3 was applied using ALD. The hard mask material was chosen since it does not re-deposit during the etch process, unlike electron-beam lithography resist. Also, a new etch chemistry of chlorine/oxygen, rather than the usual boron trichloride, aimed to increase the etch rate and improve quality in terms of smoother sidewalls.

The lateral etch needed to separate the InGaAs nanowires was achieved through a hydrochloric acid solution based process that removed the intervening InP material (Figure 7.6).

The all-around gate 'stack' was achieved through ALD coating of 10nm Al_2O_3 and conformal ALD of tungsten nitride (WN) to give the gate electrode (Figure 7.7). The source/drain electrodes were then applied (Figure 7.8).

The researchers compared the '4D' structure (3x4 NW) with '3D' single-layer 1x4 NW GAA transistors. The '1x4' consists of four lateral nanowires on the same level grouped together as transistors and '3x4' consists of 12 NWs in all, with 4 NWs each in 3 layers. The researchers also compared the transistors with the group's previous 3D devices reported at IEDM in 2011.

The new 3D devices benefited from smaller equivalent oxide thickness (EOT, 2.2nm versus 4.5nm for an older device given by 5nm and 10nm of Al_2O_3, respectively) of the gate insulating Al_2O_3 dielectric, leading to improvement in performance with respect to short-channel effects such as much reduced drain-induced barrier lowering (~50mV/V), subthreshold swing (~94mV/decade), and threshold voltage stability over different channel lengths (~–0.25V). ►

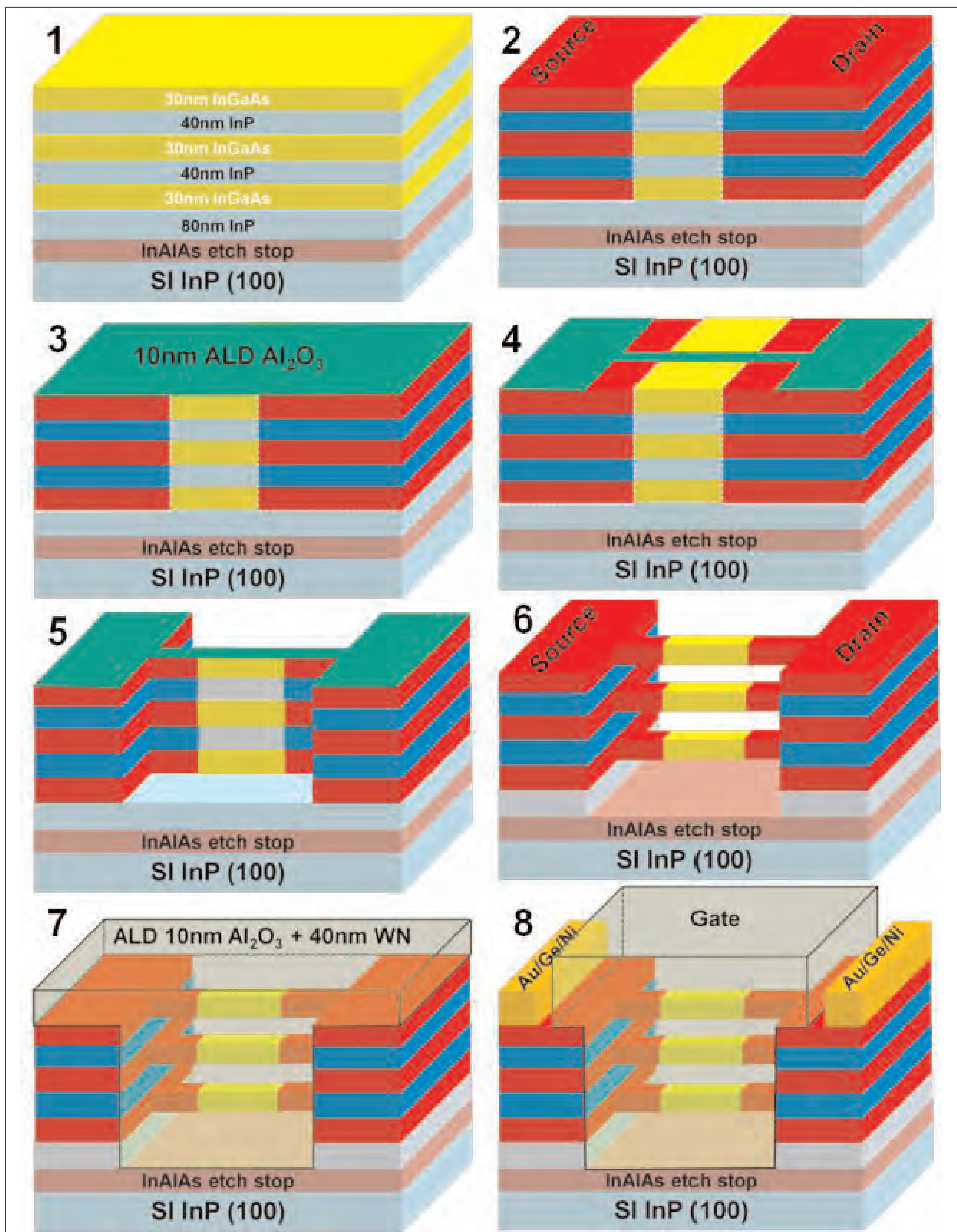

Figure 7. Schematic diagram of key process steps in the fabrication of III-V 4D transistors with three layers of InGaAs NWs stacked vertically.

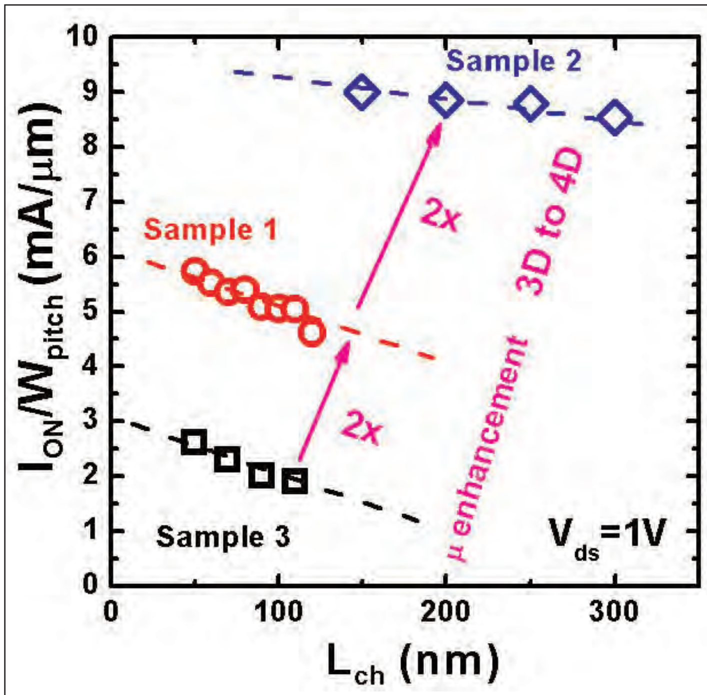

Figure 8. Benchmarking on-current (I_{ON}) normalized with respect to the maximum pitch of the nanowires in a stack (W_{pitch}) for new 3D, 4D, and old 3D transistors (samples 1-3, respectively), indicating the benefit of EOT scaling, mobility enhancement and vertical NW stacking from 3D to 4D integration.

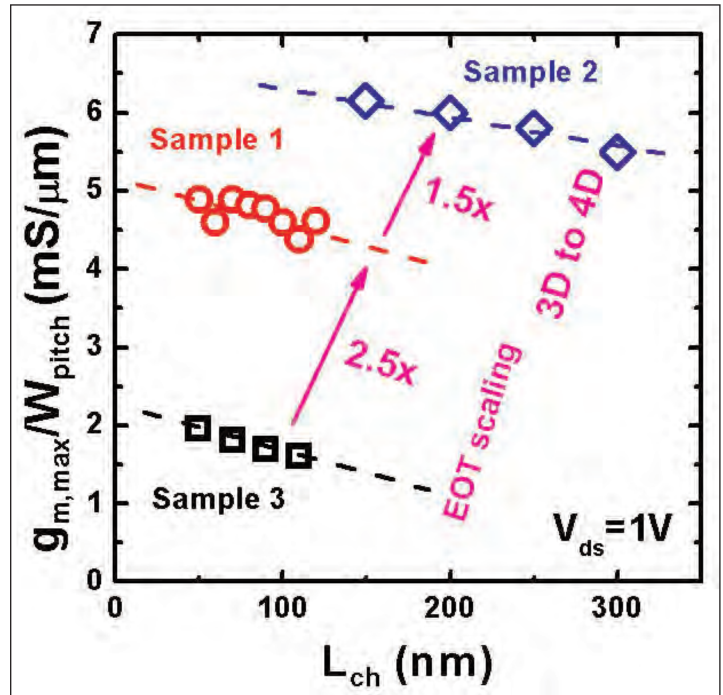

Figure 9. Benchmarking maximum transconductance (g_m) per W_{pitch} for same devices as Figure 8.

For the 4D structures (with larger EOT ~4.5nm), the main benefits were increased on-current (Figure 8) and maximum transconductance (Figure 9).

Although there are possibilities for thinner EOTs for both the 3D and 4D devices, there is a potential penalty in terms of increased gate leakage current. This was seen with the new 3D device.

Purdue and Harvard have also reduced the channel length of their 3D GAA nanowire devices to 20nm [J.J. Gu et al, session 27.6]. The on-current was 850μA/μm at 0.8V drain voltage. The peak transconductance was 1.65mS/μm at 0.5V drain. The lowest subthreshold swing was 63mV/dec and the DIBL was only 7mV/V.

Tackling gate oxide road block to Ge/III-V logic ICs

An international research team reported research into the role of gate oxide border traps in devices being developed for future electronics [D. Lin et al, IEDM 2012, session 28.3]. The work was carried out at the IMEC development center in Belgium, along with Globalfoundries and Stanford University in the USA. IMEC also worked with key partners in its core CMOS technology program: Intel, Micron, Panasonic, Samsung, TSMC, Elpida, SK Hynix, Fujitsu, Toshiba/Sandisk, and Sony.

IMEC has been developing germanium (Ge) p-channel devices on 75% localized strain-relaxed buffers of silicon germanium (SiGe). This boosted mobility by 59% compared with strained silicon buffers (Figure 10). The team studied Ge Fin field-effect transistors (FETs) that were created using a silicon replacement process which the researchers see as having potential for the 10nm and 7nm transistor nodes.

Much work on high-mobility transistors has recently focused on traps at the interface between the gate oxide insulation and the channel. These traps introduce adverse delay effects on device performance. The

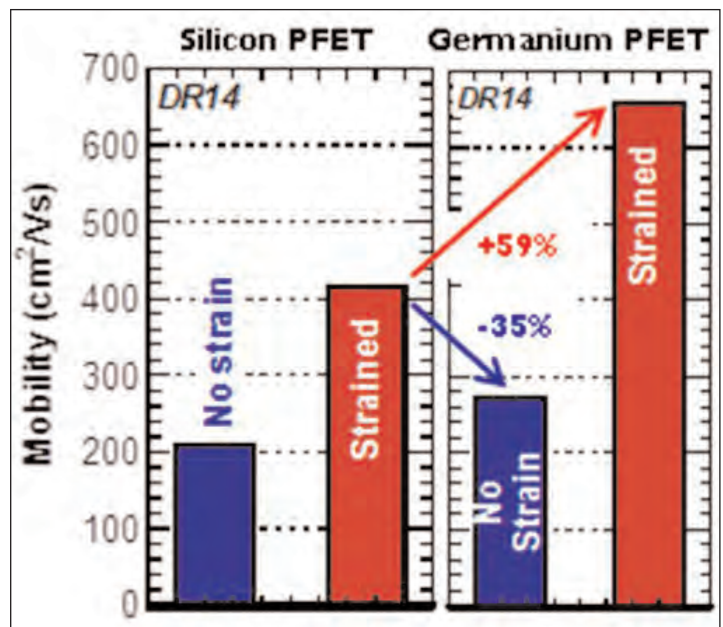

Figure 10. Comparison of mobility in unstrained and strained Si and Ge p-FinFETs, according to IMEC-led research. Unstrained Ge shows degraded mobility with respect to strained Si. Strained Ge can improve pFET mobility by 59%.

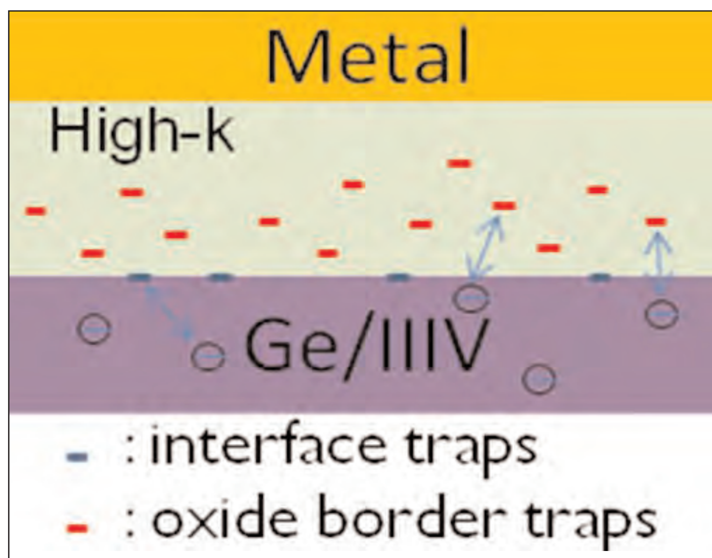

Figure 11. Without a highly insulating interfacial blocking layer (e.g. SiO_2), carriers in the channel can directly interact with border traps in high-k dielectric.

researchers say that, as a result of this work, this particular problem now appears to be contained.

The new work by IMEC et al explored the adverse impact of oxide border traps inside the oxide insulator of the metal-oxide-semiconductor (MOS) gate stack (Figure 11). Shallow, fast oxide traps have been linked to frequency-dependent transconductance effects in non-silicon MOSFETs. Such a frequency dependence can pose significant problems for circuit design using the new transistors.

The researchers also mapped out slower traps using trap spectroscopy by charge injection and sensing (TSCIS). These traps cause threshold voltages (V_T) to drift, creating problems with predicting how a circuit will perform over time. Further, the overdrive voltages (V_{ON}–V_T) for III-V (255mV) and Ge-based (212mV) transistors are expected to be about a factor of three smaller than for existing silicon-based devices, making threshold drift a much more significant problem. The lower overdrive without drift is targeted by the International Technology Roadmap for Semiconductors (ITRS) because it allows lower-voltage/power operation.

The researchers write: "This study raises the urgent issues of border traps and the need for engineering workarounds. Fundamental understandings on the nature and formation of these traps are required for long-term solutions."

Another area that the team is exploring is germanium-tin (GeSn) alloy channels, where it is hoped to develop high-mobility n- and p-channel devices in one material system. The researchers have managed to grow high-quality GeSn on Ge on Si using CVD [S. Gupta et al, session 16.2]. NMOSFETs incorporating channels with Sn content up to 8.5% were demonstrated "for the first time". Previously, GeSn PMOSFETs have been developed that outperform Ge-based devices.

Tunneling

A number of groups reported improvements of tunnel FETs (TFETs) that promise better control of sub-threshold behavior, but tend to suffer from reduced maximum drain current. Zurich-based researchers at IBM and ETH [H. Riel et al, session 16.6] reported InAs-Si vertical heterojunction nanowire tunnel diodes with record high currents of $6MA/cm^2$ at 0.5V in reverse bias and TFETs with 2.4μA/μm on-current, on/off current ratio of 10^6 and a subthreshold slope of 150mV/dec over three decades.

University of Notre Dame and IntelliEpi also reported record current densities for InGaAs/GaSb TFETs of 180μA/μm at 0.5V drain bias [G. Zhou et al, session 32.6]. The structure was again vertical and incorporated a novel gate-recess process, enabling low drain ohmic contact and access resistances. The InAs/GaSb tunnel junction features a broken band alignment. The on/off current ratio was $6x10^3$. The minimum subthreshold swing (SS) was 200mV/dec at 300K and 50mV/dec at 77K. C–V measurements indicated the subthreshold performance was degraded by a high interfacial trap density.

Gate stack developments

Finally, three groups reported gate stack developments. National Taiwan University, Taiwan's National Nano Device Laboratories, and University of California Berkeley reported low gate leakage of ~$2x10^{-3}A/cm^2$ for zirconium oxide (ZrO_2) gate insulator on Ge channel with an equivalent oxide thickness (EOT) of 0.39nm [C.-M. Lin et al, session 23.2]. The gate stack was applied to Ge pFET devices without an interfacial layer. The structure gave 104x less leakage than other reported dielectrics in the same EOT region. The subthreshold swing was ~85mV/dec and the on/off ratio was ~$6x10^5$ at –1V drain bias. A Ge nFET was also produced with SS of 90mV/dec and on/off of ~$1x10^5$ at +1V drain bias.

Taiwan Semiconductor Manufacturing Corp (TSMC) reported the first demonstration of scaled Ge p-channel FinFET devices fabricated on a Si bulk FinFET baseline using the Aspect-Ratio-Trapping (ART) technique [M.J.H. van Dal et al, session 23.5]. The subtheshold swing (SS) for long-channel devices was 76mV/dec at 0.5V drain bias. The peak transconductance (g_m) was 1.2mS/μm at 1V and 1.05mS/μm at 0.5V. The researchers comment: "The Ge FinFET presented in this work exhibits highest g_m/SS at V_{dd} = 1V reported for non-planar unstrained Ge pFETs to date."

Teledyne Scientific, UNIST and IntelliEpi have developed a three-step recess process for planar InGaAs MOSFETs that achieves, the researchers reckon, the highest value for transconductance of 2mS/μm with a 0.5V drain for any III-V MOSFETs [D.-H. Kim et al, session 32.2]. The gate stack contained an $InP/Al_2O_3/HfO_2$ composite insulator with an EOT of 0.8nm. An enhancement-mode device with a gate length of 35nm had a 0.17V threshold, DIBL of 135mV/V, and SS of 115mV/dec. ■