Nano-scale gallium oxide high-voltage transistor demonstration

Easy production of nanomembranes of wide-bandgap material motivates research towards integration into multiple platforms.

An international team of researchers has been exploring nanomembranes of beta-phase gallium oxide (β-Ga_2O_3) as a channel material for high-voltage field-effect transistors (FETs) [Wan Sik Hwang et al, Appl. Phys. Lett., vol104, p203111, 2014]. The researchers are variously associated with Korea Aerospace University, University of Notre Dame, USA, University of California Santa Barbara, USA, IBM T. J. Watson Research Center, USA, Leibniz Institute for Crystal Growth, Germany, and University of Parma, Italy.

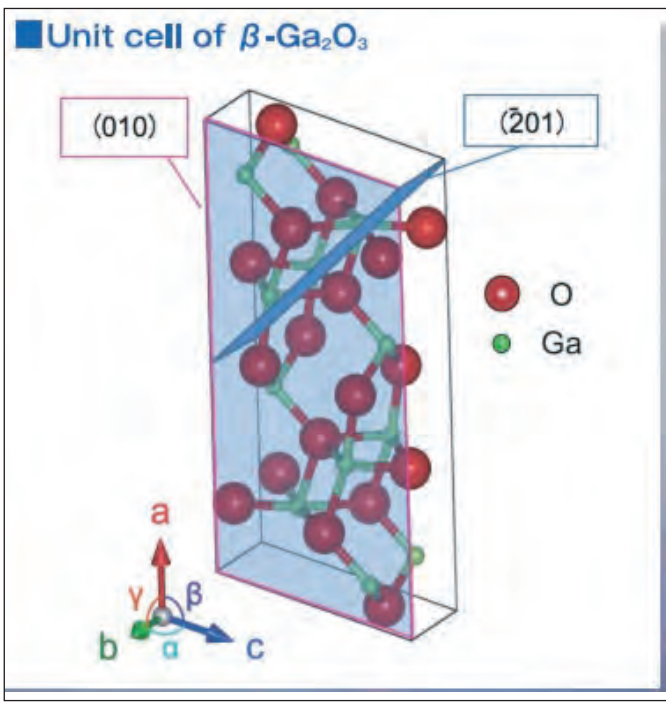
Bulk β-Ga_2O_3 has a wide bandgap energy of around 4.9eV, which should correspond to high critical fields for breakdown. This bandgap is even wider than those for materials such as silicon carbide (SiC ~3.3eV) or gallium nitride (GaN ~3.4eV) that are presently being developed for high-voltage and high-power applications.

The drawback of β-Ga_2O_3 for such applications is a low thermal conductivity of 13W/m-K, compared with 150W/m-K for Si, 150–200W/m-K for GaN, and 360–400W/m-K for SiC. For power devices, thermal management requires high thermal conductivities to enable efficient heat dissipation.

The research team believes that thin layers of β-Ga_2O_3 integrated with more thermally conductive substrates could overcome the heat dissipation problem. Such integration has been demonstrated for low-power electronics based on layered materials such as graphene and metal dichalcogenides such as molybdenum disulfide (MoS_2).

The researchers used a mechanical exfoliation technique to create nanomembranes of β-Ga_2O_3. Mechanical exfoliation with sticky tape applied to graphite is how graphene was first produced for characterization.

Although β-Ga_2O_3 does not have the layered structure of graphene that has strong in-plane covalent bonds and weak intra-plane van der Waals bonding, mechanical exfoliation nevertheless results in nanomembranes of thickness between 20nm and 100nm. The researchers suggest that, despite β-Ga_2O_3 technically being a three-dimensional crystal (Figure 1), the long



Characteristics

Crystal structure	Monoclinic a=12.23Å,b=3.04Å,c=5.8Å β=103.7°
Density	5.95×10³ kg/m³
Vickers hardness	(101): 9.7 GPa (2̄01): 12.5 GPa
Young's modulus	230 GPa
Melting point	1725°C
Thermal conductivity	[100]: 13.6 W/m · K [010]: 22.8 W/m · K
Specific heat capacity	0.49×10³ J/kg · K
Bandgap	4.8 ~ 4.9 eV
Refractive index	1.97 @450 nm

Figure 1. Crystal structure and properties from www.mtixtl.com/Ga2O3onAl2O3-101005S1-1.aspx

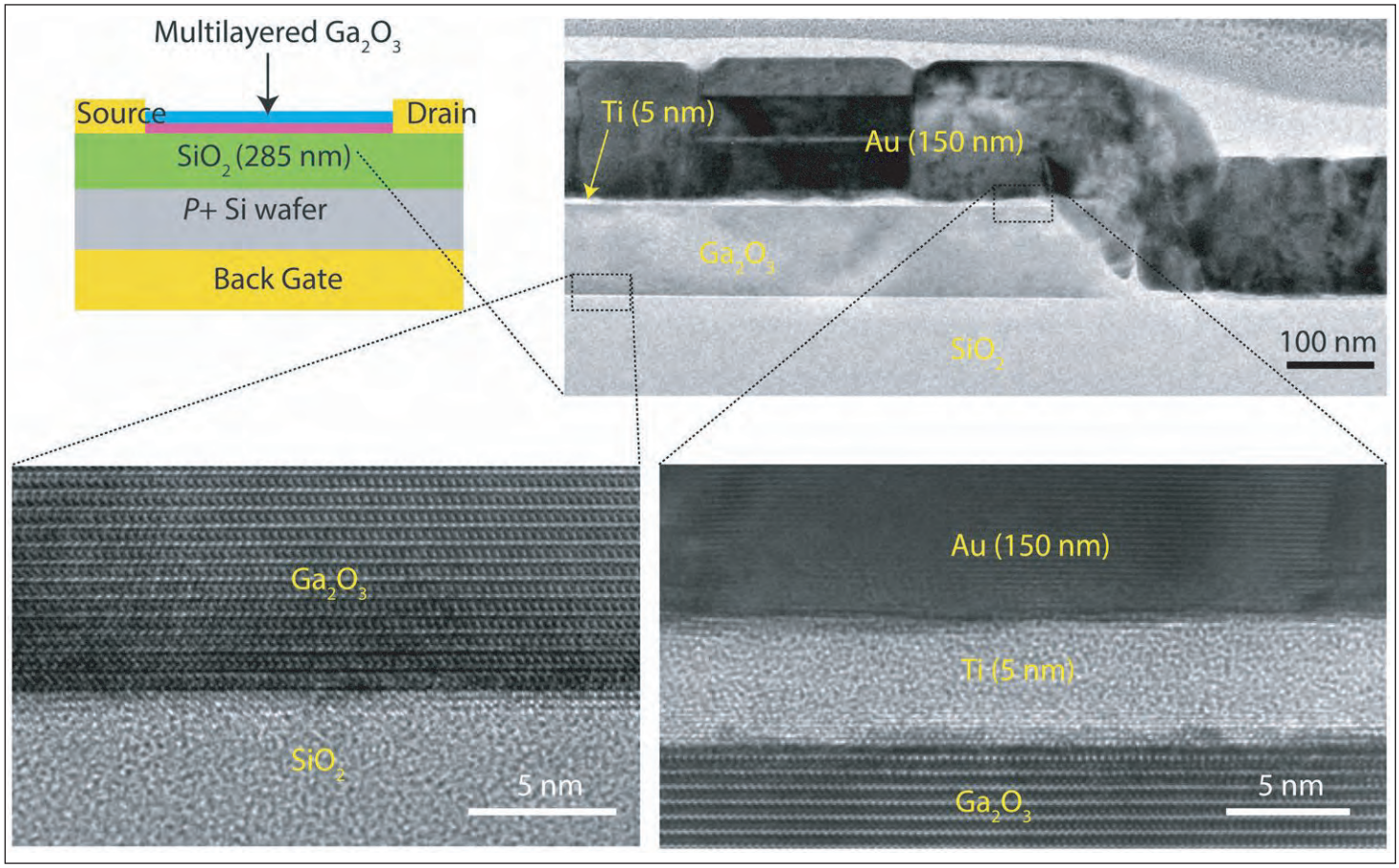


Figure 2. Cross-sectional TEM image of β-Ga_2O_3 FETs, showing a flat interface between β-Ga_2O_3 and the SiO_2 dielectrics as well as between the β-Ga_2O_3 and the Ti/Au electrode.

lattice constant in the (100) direction (a) leads to easier exfoliation than expected.

The researchers admit: "Mechanical exfoliation is indeed not a scalable method, but methods similar to smart-cut technology used in silicon-on-insulator (SOI) wafer manufacture can potentially enable controlled release of large nanomembranes of the wide-bandgap material. Such a method can potentially enable the integration of nanomembrane high-voltage transistors on multiple platforms for high-voltage switching and power management."

The 20mm-diameter single crystals of β-Ga_2O_3were produced by the Czochralski process of slowly drawing the crystal out of a melt in an iridium crucible. The melting point of β-Ga_2O_3 is 1820°C. The crystal growth was carried out in a dynamically adjusted atmosphere designed to reduce decomposition of the Ga_2O_3 while avoiding oxidation of the iridium crucible.

The researchers produced 1cm-side cubes of β-Ga_2O_3 crystal with exposed (100) planes for exfoliation and easy cleaving. Hall measurements in the Van der Pauw configuration with indium/gallium contacts gave a free-electron concentration of $5.5x10^{17}/cm^3$, mobility of $112cm^2/V\text{-}s$, and resistivity of 0.1Ω-cm.

Energy-dispersive x-ray analysis gave an optical bandgap of 4.77eV for the nanomembrane material. Band-structure calculations suggest an indirect bandgap of 4.85eV, with a slightly larger direct gap of 4.88eV at the Γ-point (k=0). The conduction-band minimum is at Γ with an almost isotropic effective mass of 0.28x the free-space mass. The valence-band maximum is located along the I–L line.

The transistor structure (Figure 2) used a back-gate. The exfoliated Ga_2O_3 nanomembrane was transferred to a thermal silicon dioxide layer on a silicon substrate. The source/drain electrodes consisted of titanium/gold annealed at 300°C for three hours in an argon/hydrogen environment. Transmission electron micrography (TEM) was used to confirm that the lattice parameters of the nanomembrane were unchanged from the bulk values "indicating minimal strain and damage in the transfer and device fabrication process". In particular, the material was unstrained in the channel, under the source/drain contacts, and at the interface with the underlying silicon dioxide.

With a high 20V drain bias, the gate was able to modulate the current by a factor of ~10^7 at room temperature. The limiting factor for the on/off current range was not the channel, but rather gate leakage. The extrinsic field-effect mobility (uncorrected for contact resistance of ~55Ω-mm) was $70cm^2/V\text{-}s$. The real 'intrinsic' mobility of the device is expected to be nearer the bulk value at ~$130cm^2/V\text{-}s$.

Although the subthreshold swing of 200mV/decade is

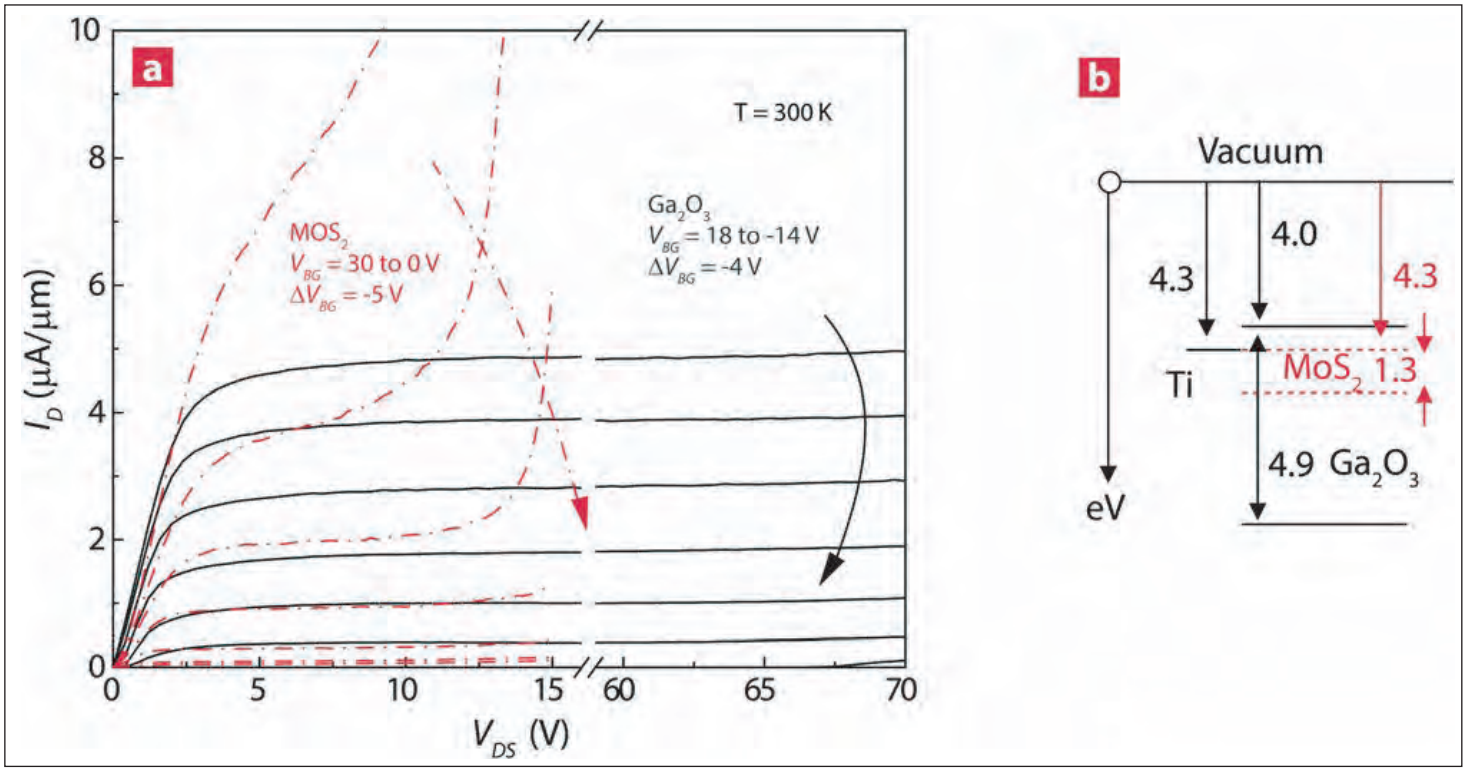


Figure 3. (a) Common-source transistor characteristics, drain current versus drain bias in linear region and current saturation under high drain bias, and comparison of breakdown voltage of β-Ga_2O_3 and MoS_2. Device widths/lengths of 1/3μm. (b) Band diagram of β-Ga_2O_3 compared with MoS_2, indicating formation of Schottky barrier contact between metal and β-Ga_2O_3.

far from the ideal 60mV/decade, the researchers comment that the value is "encouraging", given the unoptimized interfaces and the thick silicon dioxide back-gate dielectric layer. The device has an unintentional n-type (negative electron charge carriers) behavior. This could be due to atomic defects and/or impurities.

The researchers believe that the relatively high contact resistance could be improved by using metals with low workfunction or by ion implantation of dopants under the contacts. The present contact resistance performance is comparable to that obtained with MoS_2 transistors. While MoS_2 transistors tend to suffer avalanche breakdown at around 15V (Figure 3), Ga_2O_3 transistors "maintain a robust current saturation up to 70V with no signs of output conductance".

The researchers add: "This result shows that nanomembrane β-Ga_2O_3 channel transistors can sustain and switch high voltages even when integrated in thin layer forms on foreign substrates. High thermal conductivity but electrically insulating layers such as AlN or BN can be used to help circumvent the low thermal conductivity of the β-Ga_2O_3 channel. The high-thermal-conductivity insulating layers can also serve as the gate insulator for the transistor." ■

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