ALE boosts surface-channel GaAs transistor drive

The maximum drain current in GaAs NMOSFETs has been raised to a record 336mA/mm.

Researchers at Purdue and Harvard universities have developed gallium arsenide (GaAs) enhancement-mode (E-mode) surface/n-channel metal-oxide-semiconductor field-effect transistors (NMOSFETs) with a maximum drain current of 336mA/mm, which is claimed to be a record high for such devices [L. Dong et al, IEEE Electron Device Letters 34 (4) p487; published online 7 March 2013, DOI: 10.1109/LED.2013.2244058].

The performance was enabled by atomic layer epitaxy (ALE) of the gate dielectric and annealing to reduce interface trap densities. Such traps kill performance by collecting charge that shields the gate, reducing its electrostatic effectiveness.

The NMOSFETs (Figure 1) were produced from semi-insulating GaAs 2-inch wafers. The crystal orientation used was (111)A, which avoids As–As bonds on the GaAs surface. Such bonds can lead to pinning of the Fermi level, killing device performance.

Dielectric deposition followed a number of surface preparation steps designed to degrease the wafers, remove native oxide layers and passivate the surface. The ALE dielectric stack consisted of 7.5nm lanthanum yttrium oxide ($La_{1.8}Y_{0.2}O_3$) and 6.5nm aluminium oxide (Al_2O_3). The Al_2O_3 was used to protect the lower dielectric layer from reacting with water molecules from the air and from the following process steps. The equivalent oxide thickness of the structure was around 4.5nm.

Metal-organic precursors were used: lanthanum tris(N,N'-diisopropylformamidinate), yttrium tris(N,N'-diisopropyl-acetamidinate), and trimethyl-aluminium. The oxygen source was water. Atomic layer epitaxy consisted of pulsing the precursors. The chamber was purged with nitrogen after each water vapor pulse. Water molecules and/or hydroxyl groups trapped in the deposited material degrades crystallinity and dielectric permittivity.

Further fabrication consisted of implanting the source–drain regions with silicon to create n^+-type semiconductor regions. The implant was followed by rapid thermal annealing (RTA) at 860°C for 15 seconds in nitrogen for dopant activation. The metallization of the source–drain regions consisted of gold/germanium/nickel/gold stacks defined by lift-off photolithography. Ohmic contact was created through more RTA at 400°C for 30 seconds in nitrogen. Further lift-off photolithography created a nickel/gold gate electrode.

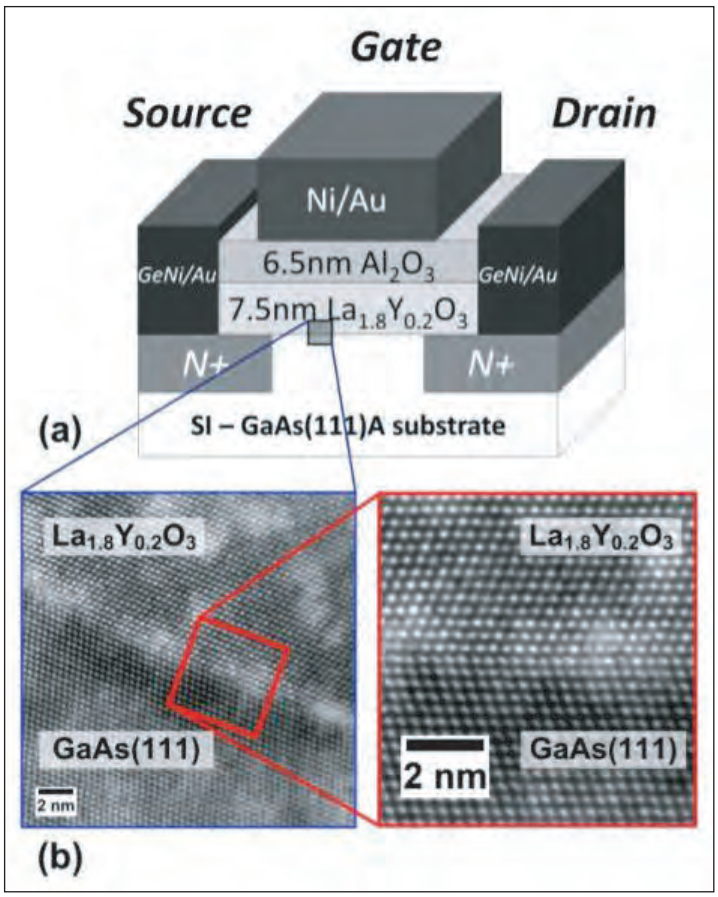

Figure 1. (a) Cross section of a GaAs(111)A surface channel E-mode NMOSFET. (b) High-resolution TEM image and enlarged view of single-crystalline GaAs–single-crystalline $La_{1.8}Y_{0.2}O_3$ interface after 860°C RTA annealing. Epitaxial $La_{1.8}Y_{0.2}O_3$ forms flat and sharp interface on GaAs(111)A substrate.

The resulting devices were 100μm wide with various gate lengths (0.5–40μm). MOS capacitors (formed in a similar way on n- and p-type substrates, but without source–drain regions) were also produced for capacitance–voltage analysis of dielectric/semiconductor interface traps.

An NMOSFET with 0.5μm-long gate had a maximum drain current of 336mA/mm (Figure 2), described as a "significant improvement of the on-state current compared with the previously reported GaAs (111)A NMOSFETs with amorphous Al_2O_3 as the gate dielectric". The peak current was achieved at 5V gate and 2V drain biases.

The researchers believe that the high quality of their

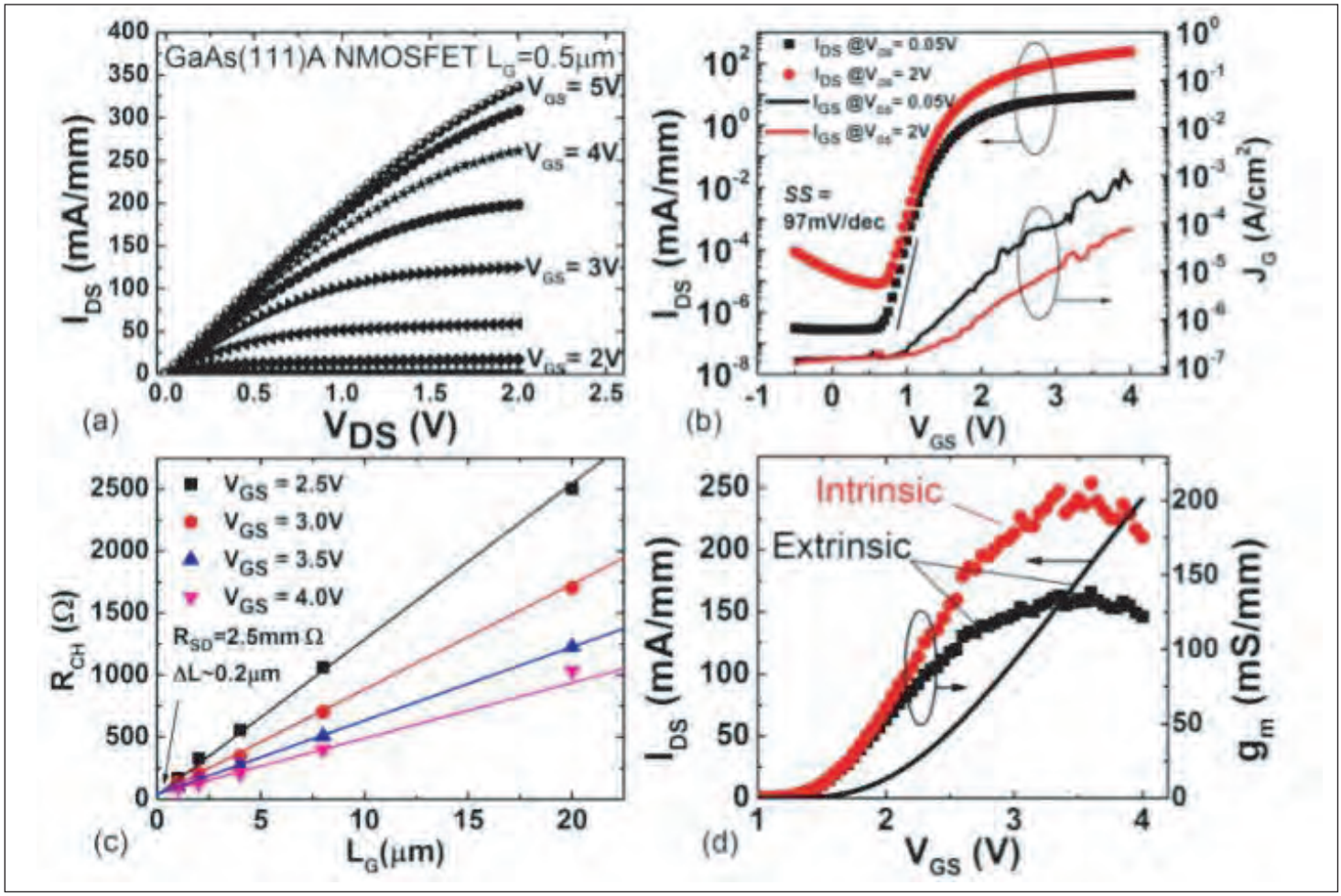

Figure 2. (a) Current–voltage (I–V) characteristic of 0.5μm-gate-length GaAs NMOSFET with ALE $La_{1.8}Y_{0.2}O_3$ oxide. (b) Transfer characteristics and gate leakage current density of same GaAs NMOSFET as (a). (c) Measured channel resistance vs different mask gate-length as function of gate bias. Source–drain resistance (R_{SD}) of 2.5Ω-mm and ~0.2μm for difference of the designed and effective gate-length (ΔL) are determined from fitting lines. (d) Extrinsic and intrinsic transconductance (g_m) and extrinsic drain current versus gate bias of the same GaAs NMOSFET in (a).

novel $La_{1.8}Y_{0.2}O_3$ epitaxial interface passivates dangling bonds on the GaAs surface, reducing the number of interface traps.

The channel mobility peaked at 310cm^2/V-s at an inversion charge density of 2x10^{12}/cm^2. The researchers believe that the drive current and mobility could be further enhanced by using buried channel structures or high-mobility channel material such as InGaAs.

The on/off current ratio was more than 10^7 with a drain bias of 2V (on = 2.3V gate, off = 0.5V gate). "This high I_{ON}/I_{OFF} ratio is a promising feature for GaAs as compared to InGaAs, since the latter usually suffers from high S/D leakage current as a result of its relatively narrower bandgap," the researchers comment.

The subthreshold swing was 97mV/dec across the range of gate lengths produced, again suggesting low interface trap densities in the mid-gap region.

The gate leakage increased from ~10^{-7}A/cm^2 to ~10^{-3}A/cm^2 as the gate bias increased from 0V to 4V. Despite this, the leakage remains at least five orders of magnitude smaller than the drain current up to 4V.

The maximum intrinsic transconductance for the 0.5μm-long gate NMOSFET was ~210mS/mm. The extrinsic value (i.e. not correcting for source-drain resistance) was ~138mS/mm. The researchers believe that the device transconductance could be further improved by reducing the dielectric thicknesses.

Capacitance measurements confirmed the importance of annealing for reducing interface trap densities from around 3x10^{12}/cm^2-eV to 5.5–7x10^{11}/cm^2-eV. The significant reduction is seen as key to realizing high performance in the surface-channel GaAs transistors.

The work at Purdue University was supported by the Air Force Office for Scientific Research (AFOSR). The work at Harvard University was performed at the Center for Nanoscale Systems (CNS), a member of the US National Nanotechnology Infrastructure Network (NNIN). ■

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