Vertical, CMOS and dual-gate approaches to gallium nitride power electronics

US research company HRL Laboratories has published a number of papers concerning III-nitride high-frequency power electronics in the past few months.

Gallium nitride (GaN) and related materials are being developed by researchers across the world for power switching and power microwave/millimeter-wave electronics. This is based on the wide bandgap and high electron mobility of GaN compared with silicon being attractive for reduced size and weight power devices operating at higher frequency. Target applications include components for radar systems, cellular base stations, and power converters.

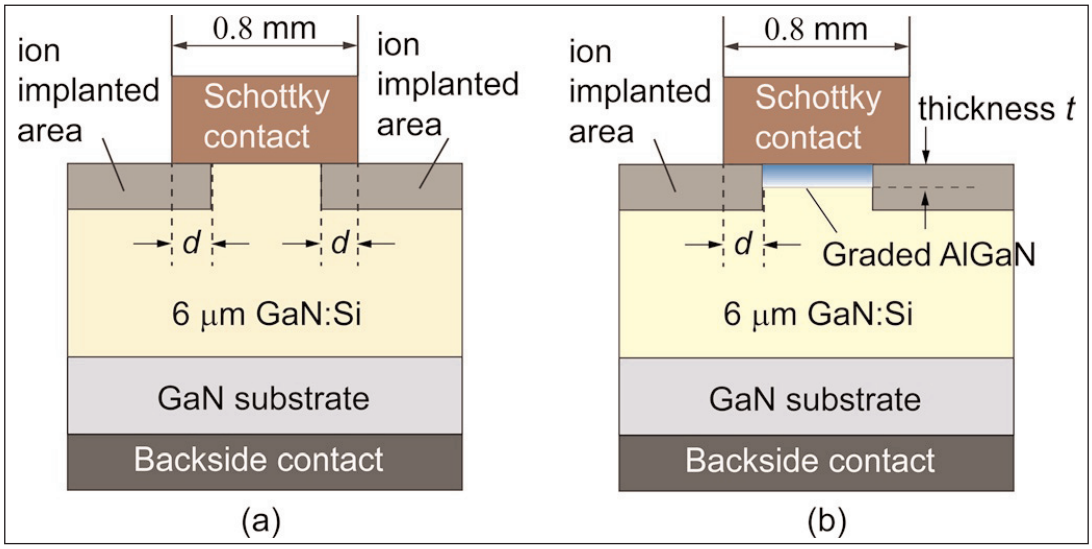

Figure 1. Schematic structures for (a) control sample A, and sample B with high doping, and (b) the sample C with graded AlGaN cap layer.

HRL Laboratories LLC in the USA is a commercial developer of GaN technology that has been making contributions to the GaN research literature for many years. In recent months, the company's research teams have published details of GaN research on vertical tunneling Schottky barrier diodes, a process for complementary metal-oxide-semiconductor (CMOS) circuits, and dual-gate high-electron-mobility transistors (HEMTs).

In addition to research, HRL provides GaN and indium phosphide foundry, monolithic microwave integrated circuit (MMIC), machine shop, and 'open innovation' research partnership services. The company has also developed a range of power amplifiers capable of handling up to 105GHz.

Here we look at HRL's recent work mentioned above.

Vertical Schottky diode

Vertical Schottky diodes and other power devices built using GaN technology could lead to higher current density handling and smaller components compared with the lateral structures that have been the focus of most development until recently.

HRL has developed a GaN vertical tunneling Schottky barrier diode (TBS) that gives good combined on and off performance, compared with vertical Schottky barrier diodes (SBDs) [Y. Cao et al, Appl. Phys. Lett., vol108, p112101, 2016], building on previous work [Y. Cao et al, Appl. Phys. Lett., vol108, p062103, 2016; reported in Semiconductor Today 2016 issue 2 (March), p90].

Gallium vertical SBDs suffer from trade offs between on-current and reverse bias breakdown. By applying a thin layer of aluminium gallium nitride (AlGaN) as a tunneling barrier, the HRL team allowed a more highly doped drift layer to be used, increasing on-current without compromising the breakdown voltage.

The new interest in vertical structures has been enabled by reductions in defect densities due to the commercial availability of free-standing and bulk GaN substrates. However, the initial work has largely been on p–n junction diodes that have high turn-on voltages of ~3V arising from the wide bandgap (~3.4eV). Devices with high turn-on voltage suffer from large conduction losses.

SBD structures can reduce turn-on to less than 1V, but usually with lower breakdown voltages. SBDs also have faster performance.

The drift layer of the HRL devices (Figure 1) was 6μm silicon-doped GaN, grown by metal-organic chemical

vapor deposition (MOCVD) at 1040ºC. The substrate was 2-inch c-plane free-standing bulk n-GaN. The carbon concentration was reduced to less than $3x10^{15}/cm^3$ by using a growth pressure of 300Torr and a V/III precursor ratio of 4777.

The tunnel barrier consisted of a 5nm graded AlGaN layer with Al-concentration varying from 0% to 23%. This was achieved by linearly ramping the flow of trimethyl-aluminium precursor.

Edge-termination of the SBDs was achieved with ion implantation. The edge-termination region overlapped 10μm with the 0.8mmx0.8mm nickel/gold Schottky contact. A non-alloyed ohmic contact was applied to the back-side of the wafer.

Two SBDs were produced with different silicon-doping levels of the drift layer (A and B): $\sim 1x10^{16}/cm^3$ and $\sim 3x10^{16}/cm^3$, respectively. The tunneling SBD (TBS), sample C, had the same silicon doping as sample B.

The TBS allowed a higher on-current compared with sample A, while maintaining good breakdown performance under reverse bias (Figure 2, Table 1).

The HRL researchers compare their TBS device with the performance of Cree's commercial silicon carbide (SiC) junction barrier Schottky diode (JBS, Table 2): "It can be seen that with a slightly smaller area, our TBS diode could achieve twice the on current of the JBS diode at V_f = 1.6V, or reach the same on current of 1A at a 28% lower forward bias. This result indicates that it is possible for a GaN-based Schottky diode to further reduce the conduction loss and improve the efficiency in current 600V systems, where SiC-based diodes are used."

SiC has similar material properties to GaN of wide bandgap and high electron mobility.

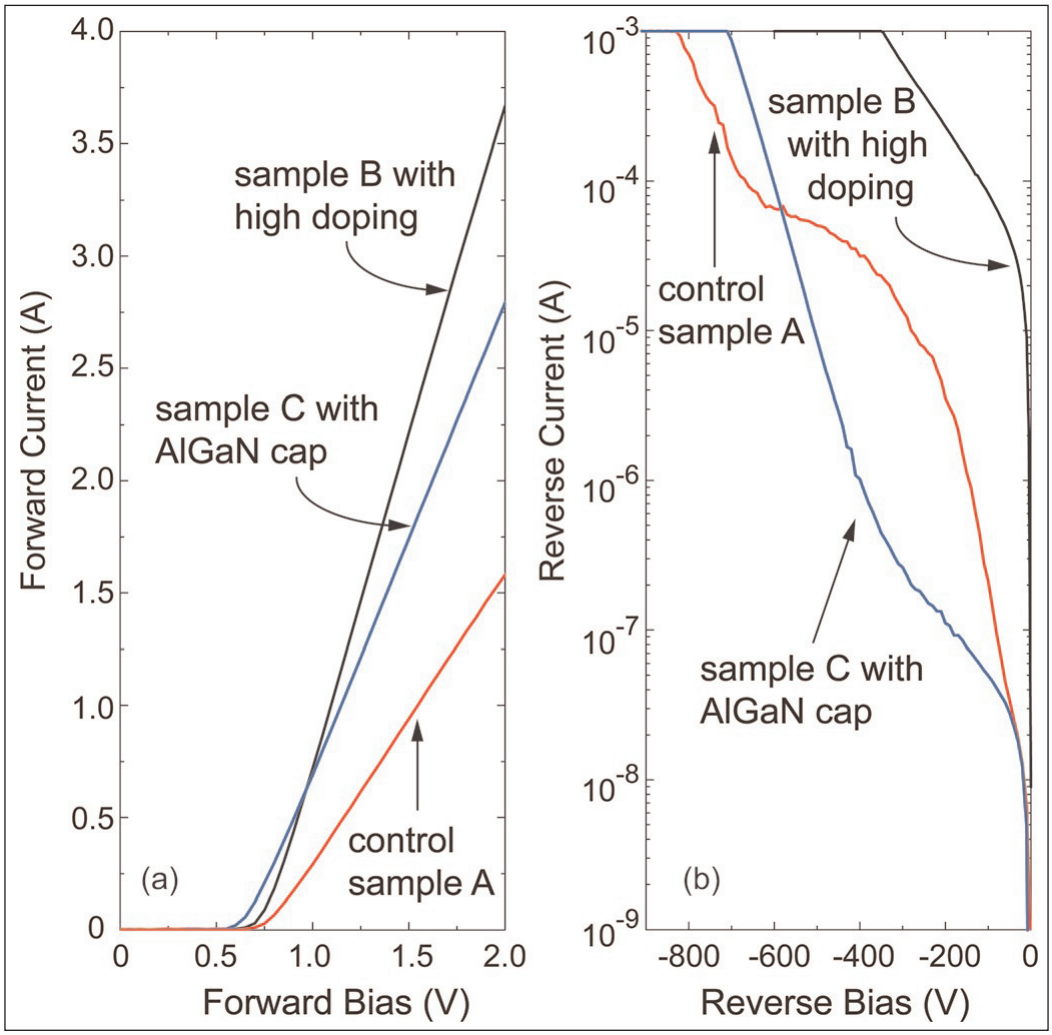

Figure 2. Forward current (a) and reverse current (b) as a function of bias.

Table 1. Performance metrics for HRL vertical Schottky diodes.

Sample	A	B	C (TBS)
Free electron density	$\sim 7.5x10^{14}/cm^3$	$2.6x10^{15}/cm^3$	$2.9x10^{15}/cm^3$
Current (I_{on}) at 1.6V forward voltage (V_f)	1.07A	2.51A	1.95A
Reverse bias breakdown at 1mA	>800V	~345V	700V
Turn-on voltage	0.77V	0.75V	0.67V
Total specific on resistance	4.94mΩ-cm^2	2.17mΩ-cm^2	3.06mΩ-cm^2

Table 2. Comparison of key parameters between HRL's tunneling barrier Schottky diode and Cree's 600V JBS.

	Die area (mm^2)	I_{on}(A) @V_f =1.6V	V_f(V) @I_{on}=1.0A
HRL GaN TBS	0.64	2.0	1.15
Cree SiC JBS (CPWR-0600S001)	0.71	1.0	1.6

CMOS fabrication

Moving to lateral devices, HRL claims the first demonstration of GaN (CMOS) field-effect-transistors [Rongming Chu et al, IEEE Electron Device Letters,

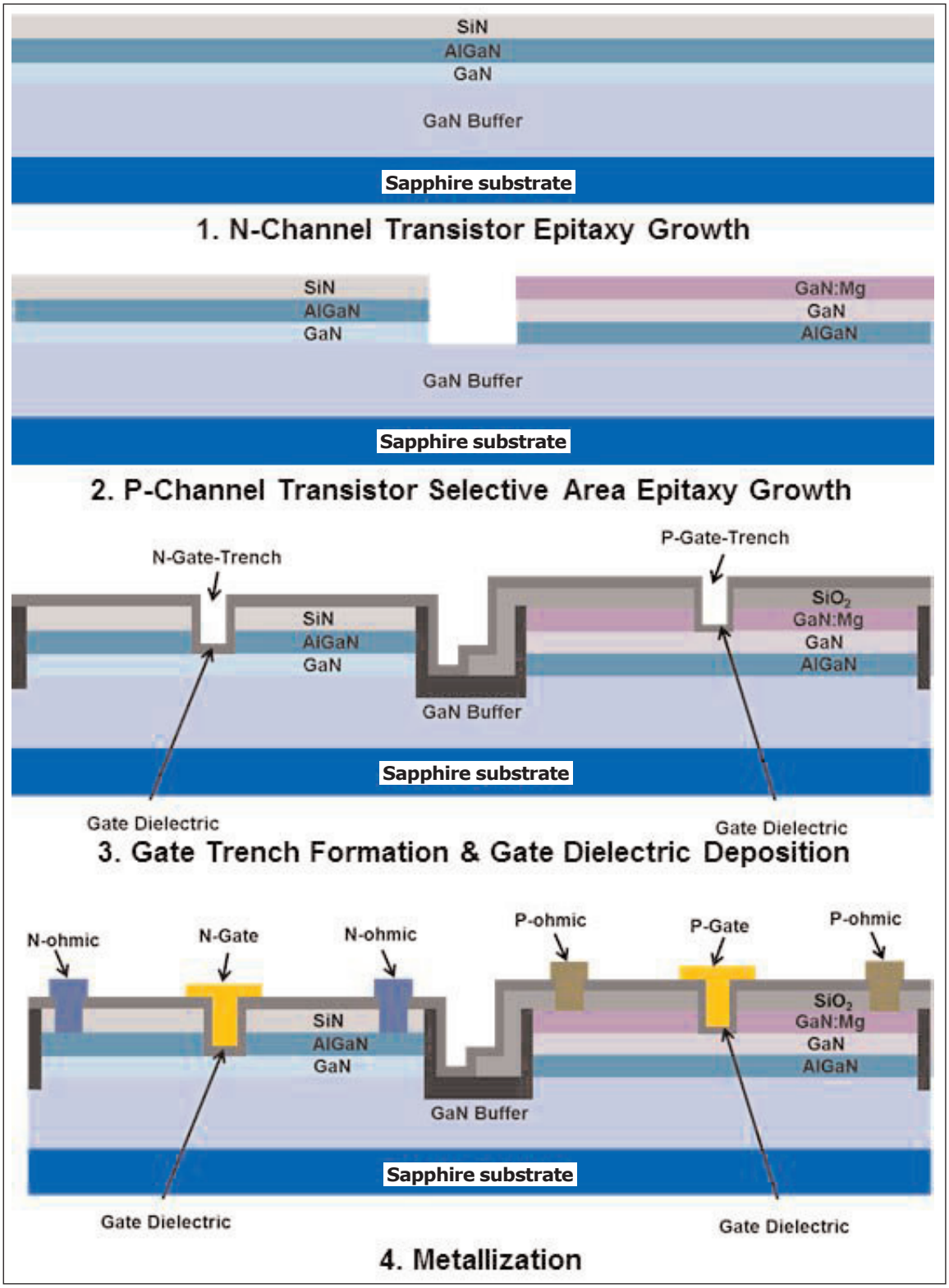

Figure 3. Major steps for fabricating GaN NMOS and PMOS on the same wafer.

published online 6 January 2016]. The team used the technology to create CMOS inverter circuits.

Present applications mostly use discrete transistors rather than integrated circuits (ICs). HRL sees a need for an IC approach to achieve the full benefits of GaN electronics at low cost. Parasitic inductance is one aspect that would be improved — discrete GaN components have to be slowed down to avoid voltage instability from chip-to-chip effects. ICs also have reduced assembly and packaging costs.

Dr Rongming Chu, HRL senior staff research engineer and principal investigator, comments: "In the near term, GaN CMOS IC applications could include power integrated circuits that manage electricity more efficiently while having a significantly smaller form factor and lower cost, and integrated circuits that can operate in harsh environments." Longer term, he believes, GaN CMOS has the potential to replace silicon CMOS in a wide range of products.

The GaN CMOS processing began with MOCVD of the NMOS layers on sapphire (Figure 3). The $Al_{0.25}Ga_{0.75}N$ top barrier was 5nm thick. The silicon nitride (SiN) encapsulation was 50nm.

The PMOS layers were applied by etching down to the GaN buffer in selected regions and MOCVD re-growth. The structure consisted of a 30nm $Al_{0.25}Ga_{0.75}N$ back barrier, 20nm of undoped GaN and a 50nm magnesium-doped GaN hole supply layer.

Transistor fabrication began with ion implantation for device isolation, followed by gate trench low-energy plasma etch, AlN/SiN gate dielectric stack MOCVD, titanium/aluminium-based NMOS and nickel/gold PMOS ohmic source/drain formation, and nickel/gold gate electrode and interconnect deposition. The PMOS source/drain contacts were annealed in oxygen.

The researchers report that the NMOS and PMOS structures both exhibited enhancement-mode behavior

in long gate devices — i.e. normally-off at 0V gate potential, which is desired in power devices for fail safety and efficiency. The channel mobilities were 300cm^2/V-s and 20cm^2/V-s for NMOS and PMOS, respectively.

The researchers report that discrete NMOS devices with the same gate stack structure have achieved channel mobilities of more than 1000cm^2/V-s. The team comments: "Further improvement of the GaN CMOS process is needed to improve the NMOS mobility to what was achievable with a discrete device process."

The PMOS mobility was higher than for bulk p-GaN (~10cm^2/V-s) but lower than reported values for two-dimensional hole gases (2DHGs, ~40cm^2/V-s). The researchers believe that PMOS improvements could come from "optimizing epitaxial regrowth, gate trench etch, and gate dielectric deposition".

Devices with 0.5μm and 75μm respective gate length and width had threshold voltages around 0V. For the NMOS device the on-resistance at +5V gate was 10Ω-mm. The PMOS on-resistance was much higher: 1314Ω-mm at –5V gate. The PMOS device also suffered from buffer leakage when the drain bias was greater than 2V. The researchers suggest that the leakage could be caused by

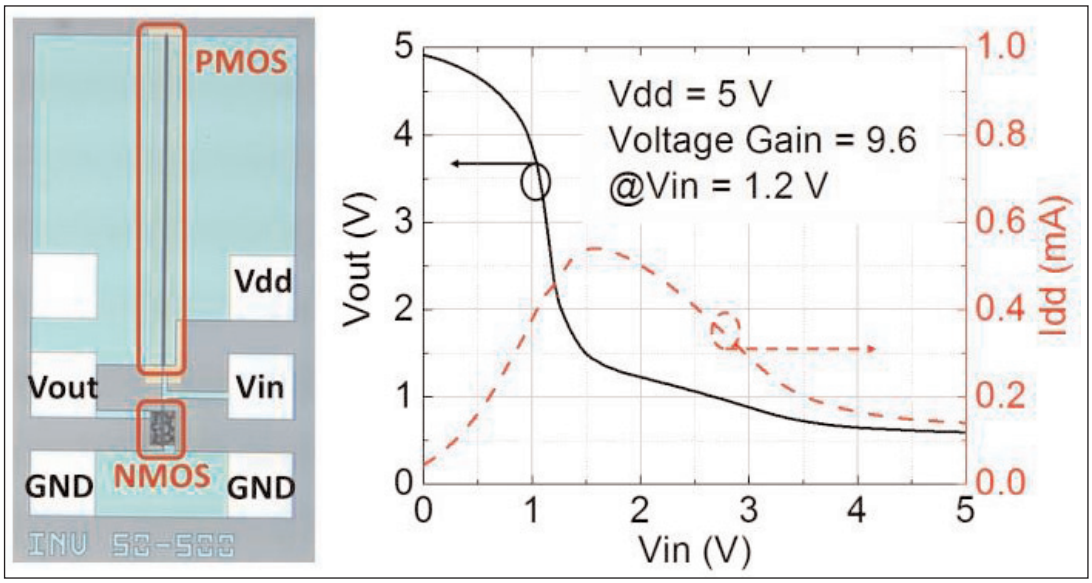

Figure 4. Microscope top-view photograph and measured voltage transfer curve of fabricated GaN CMOS inverter IC.

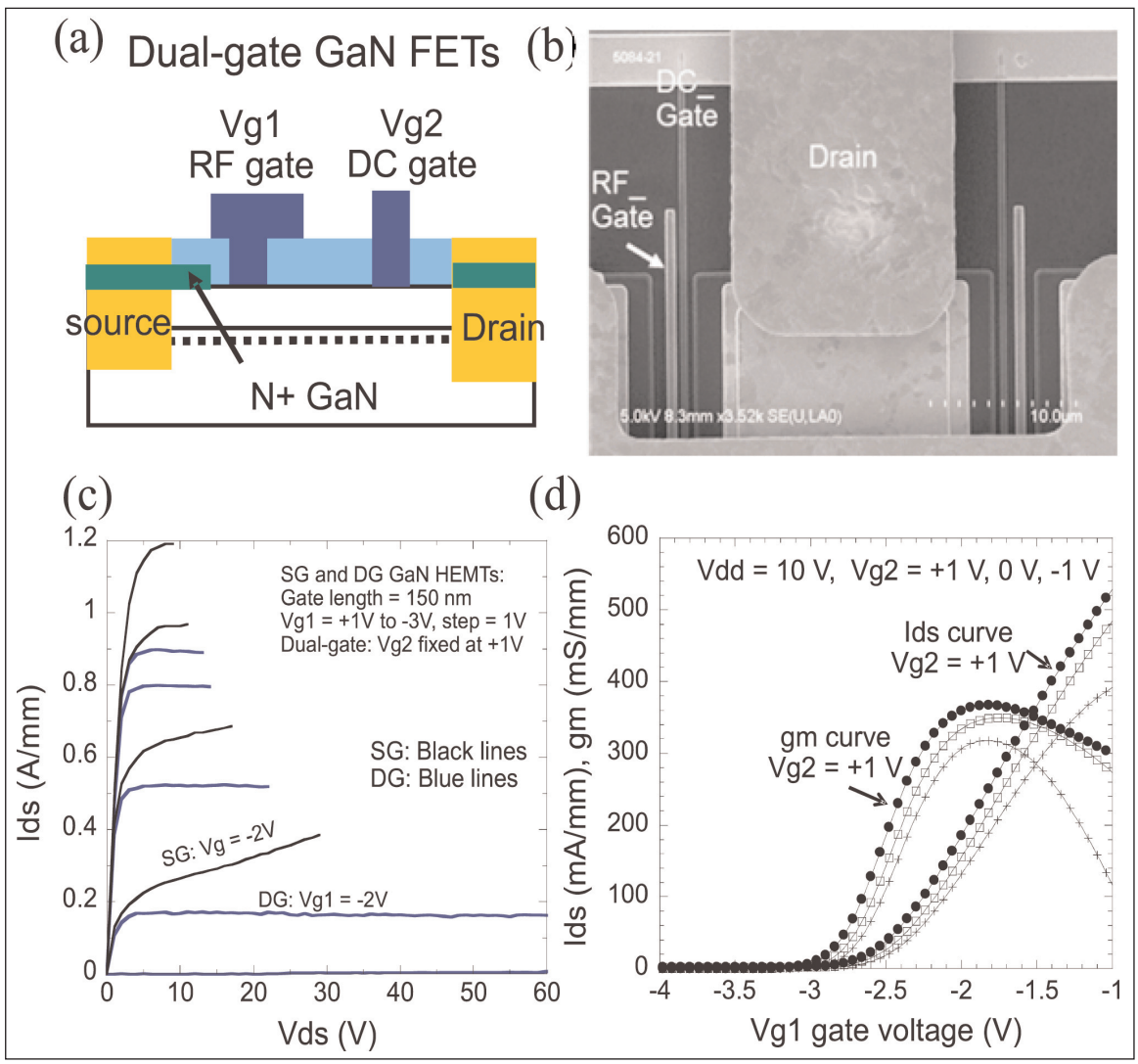

Figure 5. (a)–(b) A schematic diagram of dual-gate field-plated GaN HEMT with a 0.5μm-long n$^+$ source ledge is shown with an SEM photograph. (c) Measured pulsed current–voltage (I–V) curves of single-gate (SG) and dual-gate (DG) devices with 250ns pulses, where output conductance of DG device is greatly reduced, and (d) transfer curves of 4x37.5μm dual-gate field-plated GaN HEMT.

parallel conduction at the MOCVD re-growth interface between the PMOS layer and the original GaN buffer.

The 0.5μm transistors were used in CMOS inverter circuits (Figure 4). The gate widths of the PMOS and NMOS transistors were 500μm and 50μm, respectively. The (differential) voltage gain was 9.6 at 1.2V input with 5V DC bias. The current drawn by the circuit (I_{dd}) peaked at 1.5V input (V_{in}), where the inverter switched off.

The researchers comment: "Thanks to the CMOS configuration, the I_{dd} was considerably lower when the V_{in} was at 0V and 5V, suggesting low static power consumption. The static power consumption could be further decreased by reducing the off-state leakage of the NMOS and PMOS."

With 5V pulses with steps of 10ns rise/fall times, the output swung between 0V and ~5V with 90ns fall time and 670ns rise time.

The researchers comment: "Slower rise time is due to higher on-resistance of the PMOS. Although the performance is yet to be improved, the functional inverter IC proves the feasibility of the GaN CMOS technology."

Dual-gate HEMTs

Finally, HRL has used dual-gate and cascode GaN HEMTs to achieve power-added efficiency (PAE) figures in the 8.0–12.0GHz X-band close to the theoretical maximum of 78.5% [J. S. Moon et al, IEEE Electron Device Letters, vol. 37, p272, 2016]. The team writes: "The technology offers record performance for combined PAE, output power, and gain among reported GaN HEMTs in the X-band."

The researchers used dual-gate HEMTs with field plates (FP) on semi-insulating SiC (Figure 5). The source–drain distance was 3μm. The source–drain ohmic electrodes were titanium/aluminium. The gates for the RF signal was 150nm long. The DC gate was 250nm. The gates were recessed with ~15nm AlGaN between the electrode and channel.

The dual-gate devices are seen as being equivalent to cascode pairs of transistors, one with common-gate connected in series to one with a common-source. Previous reports of GaN HEMT cascode circuits demonstrated PAE values up to 45% at 8.2GHz, along with 3.5W/mm power density and 12dB associated gain.

The epitaxial material had a double heterojunction to give a back barrier: $Al_{0.3}Ga_{0.7}N/GaN/Al_{0.04}Ga_{0.96}N$. There was also a 0.5μm n^+-GaN cap layer, which was used to create a ledge on the source side to improve access to the channel.

The devices had surface passivation consisting of 75nm of silicon nitride, which also provided support for the field plates. The gates consisted of platinum/gold. The RF gate had a 550nm overhang to effect the field plate.

In Maury load-pull measurements at 10GHz without harmonic tuning, the devices demonstrated 13.7dB power gain at peak power added efficiency of 71%. The linear gain was 17dB. Comparison single-gate HEMTs with 2.5μm source–drain gap and field plates had 13dB power gain at peak PAE of 67%, and 16dB linear gain. The output power of both devices was about 27.4dBm (0.55W).

Cascode connected GaN HEMT pairs performed similar to the dual-gate device with ~13.4dB associated power at PAE of 71–74%. These PAE values are the highest PAE reported in GaN HEMTs at 10GHz with a few Watt level output power. The peak output power was 2.3–2.5W.

The researchers attribute a more than 10% PAE improvement of dual-gate and cascode GaN field-plate HEMTs over single-gate devices at 2W output power (33dBm) to "improved output resistance, gain, and pinch-off characteristics" (Figure 6). ■

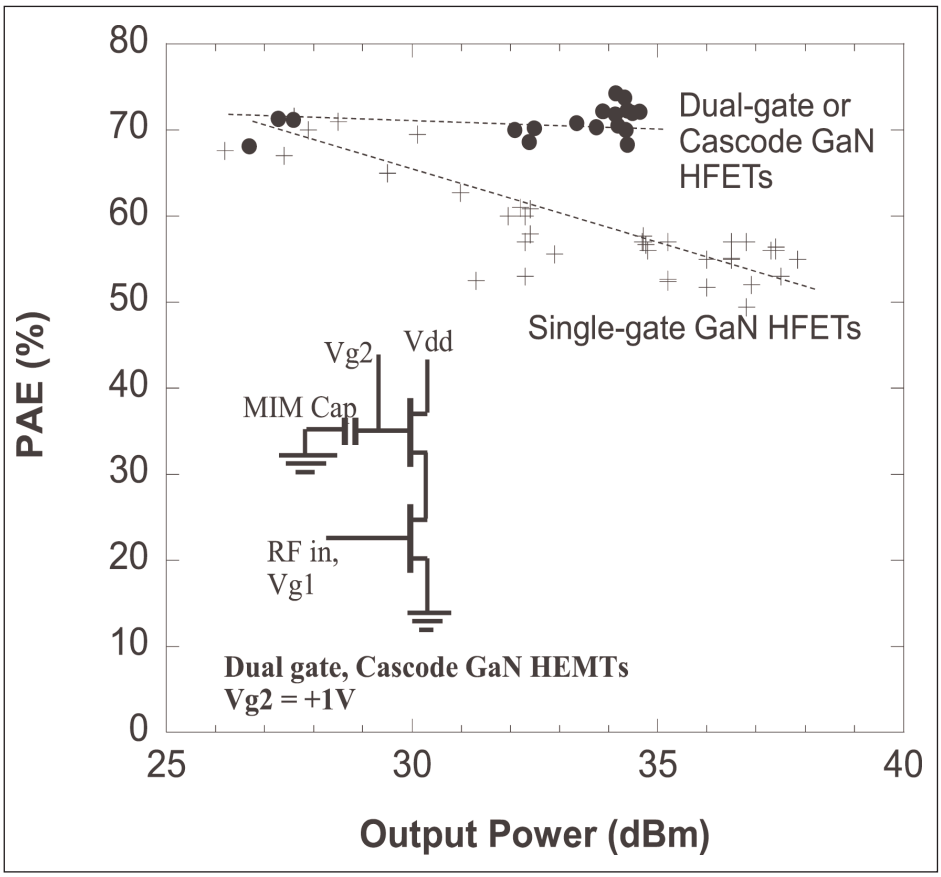

Figure 6. Measured PAE versus output power of GaN HEMTs at 10GHz without harmonic tuning.

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.