Advancing high-frequency and high-power electron device technology

Mike Cooke reports on work presented at the IEEE International Electron Devices Meeting (IEDM) in December.

The microelectronics industry is always looking forward to new technologies. The IEEE International Electron Devices Meeting (IEDM) forms an end-of-year report on progress towards many potential futures. Here we look at some of the achievements centered on III–V materials presented at the 62nd IEDM in San Francisco, USA (3–7 December 2016).

InGaAs transistors

Lund University reported on indium gallium arsenide (InGaAs) tri-gate metal-oxide-semiconductor field-effect transistors (MOSFETs) [session 3.2] and vertical tunneling field-effect transistors (TFETs) on silicon [session 19.1]. The research team for the two pieces of work were different but did overlap in senior personnel.

The tri-gate MOSFET team claimed a record on-current (I_{on}) of 650μA/μm for its devices at 0.5V operation, compared with state-of-the-art III–V planar and non-planar MOSFETs (Figure 1). The off current (I_{off}) was 100nA/μm.

The devices were based on nanowires of $In_{0.85}Ga_{0.15}As$ formed by selective-area metal-organic chemical vapor deposition (MOCVD) growth on indium phosphide (InP) using a hydrogen silsesquioxane (HSQ) mask. A device with 75nm-long gate and 25nm nanowire width achieved subthreshold swings (SSs) as low as 66mV/decade and 61mV/decade at drain biases of 0.5V and 0.05V, respectively. The drain-induced barrier lowering (DIBL) was 65mV/V with drain current density of 1μA/μm, with the gate width being the three sides of the trigate.

A quality factor given by the ratio of the maximum transconductance (3mS/μm) over the subthreshold swing (66mV/decade) of 45 (units = (S-decade)/(V-mm)?) is also claimed as a record.

Moving on to Lund's vertical nanowire TFETs, as non-planar devices, dependent on band-to-band tunneling, they were able to access SS values below the 60mV/decade room-temperature limit for planar devices, dependent on thermionic emission effects.

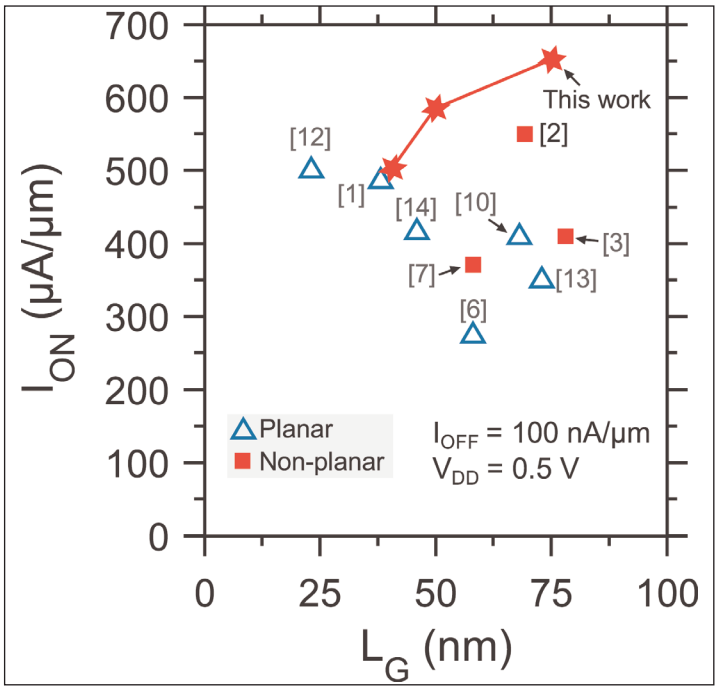

Figure 1. Benchmark at 0.5V and I_{off} = 100nA/μm.

The 0.31μA/μm current level where SS was 60mV/decade was claimed by the researchers as a record high. The minimum value achieved was 48mV/decade. With a drain bias of 0.3V, the on-current was 10μA/μm and the off-current 1nA/μm.

The nanowire positions were defined by 40nm-diameter gold disks of 15nm thickness in arrays with 1.5μm spacing. The disks were patterned using electron-beam lithography. The substrate was a 260nm layer of highly doped InAs on high-resistivity (111) silicon. The nanowires included III–antimonide (III–Sb) compound semiconductor sections.

The gold disks constituted seeds for the metal-organic vapor phase epitaxy (MOVPE) growth of 200nm/100nm/300nm InAs/p-GaAsSb/p-GaSb nanowires. The bottom 100nm of the InAs part of the nanowire was doped n-type. The top, undoped section of InAs formed the channel of the fabricated TFETs.

The InAs section of the nanowire was selectively thinned from 40nm to 20nm diameter using digital etching cycles of ozone oxidation and citric acid. The etching had no noticeable effect on the p-GaSb section, but the p-GaAsSb was thinned from 35nm to 22nm.

TFETs (Figure 2) were fabricated with atomic layer deposition (ALD) of 1nm aluminium oxide (Al_2O_3) and 4nm hafnium dioxide (HfO_2) gate insulator, evaporation deposition of 15nm silicon dioxide (SiO_2) gate–drain spacer, sputtering of 60nm tungsten (W) that was etched into 260nm long gates, spin coating of organic material as gate–source spacer, and the formation of nickel/gold (Ni/Au) contact pads.

By reducing drain bias to 0.05V, the subthreshold swing could be reduced to 44mV/decade. The minimum SS with 1V drain bias was weakly temperature dependent, increasing from 38mV/decade to 54mV/decade between 223K and 323K. "This change is smaller than the one expected from thermionic emission, which further confirms that direct band-to-band tunneling is the dominant transport mechanism in these devices," the researchers comment.

University of Tokyo and JST–CREST reported on the use of lanthanum oxide (La_2O_3) as a gate insulator for InGaAs MOSFETs [session 12.5]. The team found that La_2O_3 gate insulation resulted in lower SS with 93mV/decade minimum and lower carrier trapping at interfaces than with Al_2O_3 or HfO_2. However, a 3x higher fixed oxide charge density in the La_2O_3/InGaAs interfaces gave lower channel mobility.

The epitaxial InGaAs material was grown on InP by MOVPE. The MOSFETs were fabricated through a gate-last process and source–drain Si ion implantation. The La_2O_3 was deposited by an ALD process with (tris(isopropylcyclopentadienyl)lanthanum ($La(iPrCp)_3$) and water (H_2O) precursors. The gate was W. The post-metal anneal temperature was 300ºC.

The researchers also claimed to have found for the first time ferroelectric behavior of the W/La_2O_3/InGaAs MOS structure. The ferroelectricity was revealed as counterclockwise hysteresis in capacitance–voltage (C–V) and polarization-electric field curves when the La_2O_3 thickness exceeded 10nm. Similar behavior was seen in W/La_2O_3/W metal–insulator–metal structures.

With 15nm La_2O_3 gate insulator, negative capacitance (NC) FETs were realized. A reduction in SS to 82mV/decade is attributed to the ferroelectricity. The researchers comment: "The steep slope characteristics due to the NC effect have been demonstrated, for the first time, in W/La_2O_3/InGaAs MOSFETs, which is very promising for realizing high-I_{on} and small-SS logic applications."

Korea Institute of Science and Technology (KIST), Kookmin University, and Korea Advanced Nanofab Center (KANC) reported on a cost-effective epitaxial lift-off (ELO) process for creating monolithic $In_{0.53}Ga_{0.47}As$ layers on silicon [session 25.4]. The team hopes that its method could contribute to incorporation of III–V devices in monolithic three-dimensional electronic structures on silicon, reducing signal delays and increasing transistor density.

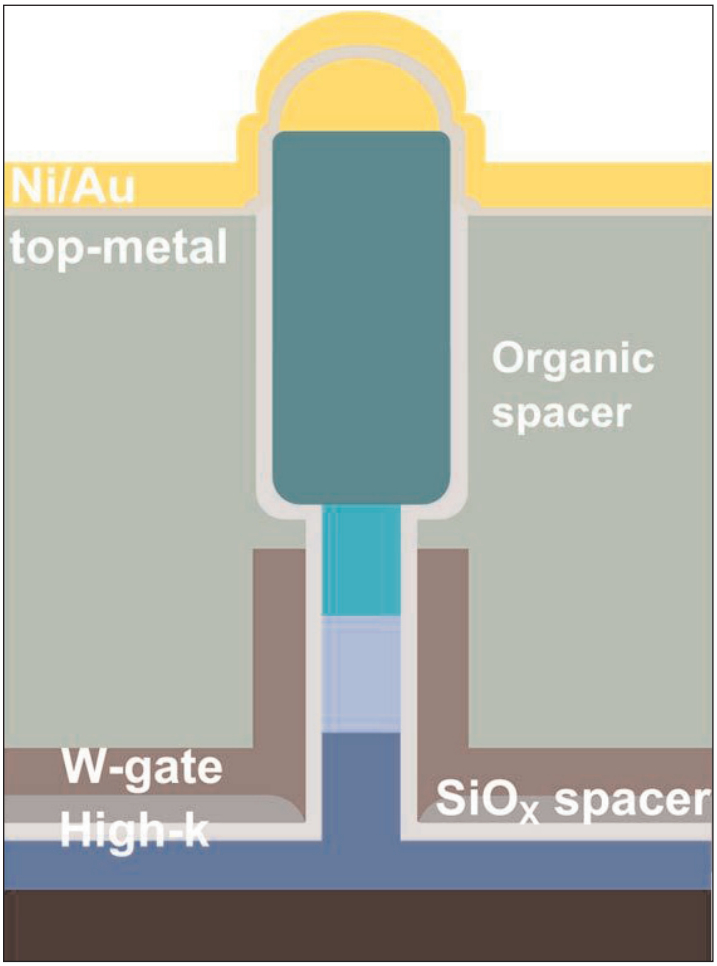

Figure 2. Schematic of InAs/GaAsSb/GaSb TFET.

The 20nm InGaAs layers were grown on AlAs sacrificial layers on InP (100). Direct wafer bonding (DWB) between the InGaAs and Si was made through 20nm yttrium oxide (Y_2O_3) layers on both surfaces. This gives an InGaAs on insulator (InGaAs-OI) structure.

The surface of the donor wafer containing the InGaAs layer was patterned to enable faster epitaxial lift-off through enlargement of the exposed area for undercutting and efficient release of gas bubbles from the AlAs hydrofluoric acid etch process. The typical area of the patterned sections was 100μmx100μm. While the InGaAs surface left by the release process was quite rough, this could be smoothed to 0.22nm root-mean-square roughness by cleaning with hydrochloric acid. A 40% reduced ELO time was enabled by a 1V electrical bias between the etch solution and target bonded wafer.

The researchers used the material to fabricate MOSFETs with 120mV/decade SS and an on/off current ratio of more than 10^6. The researchers believe these values

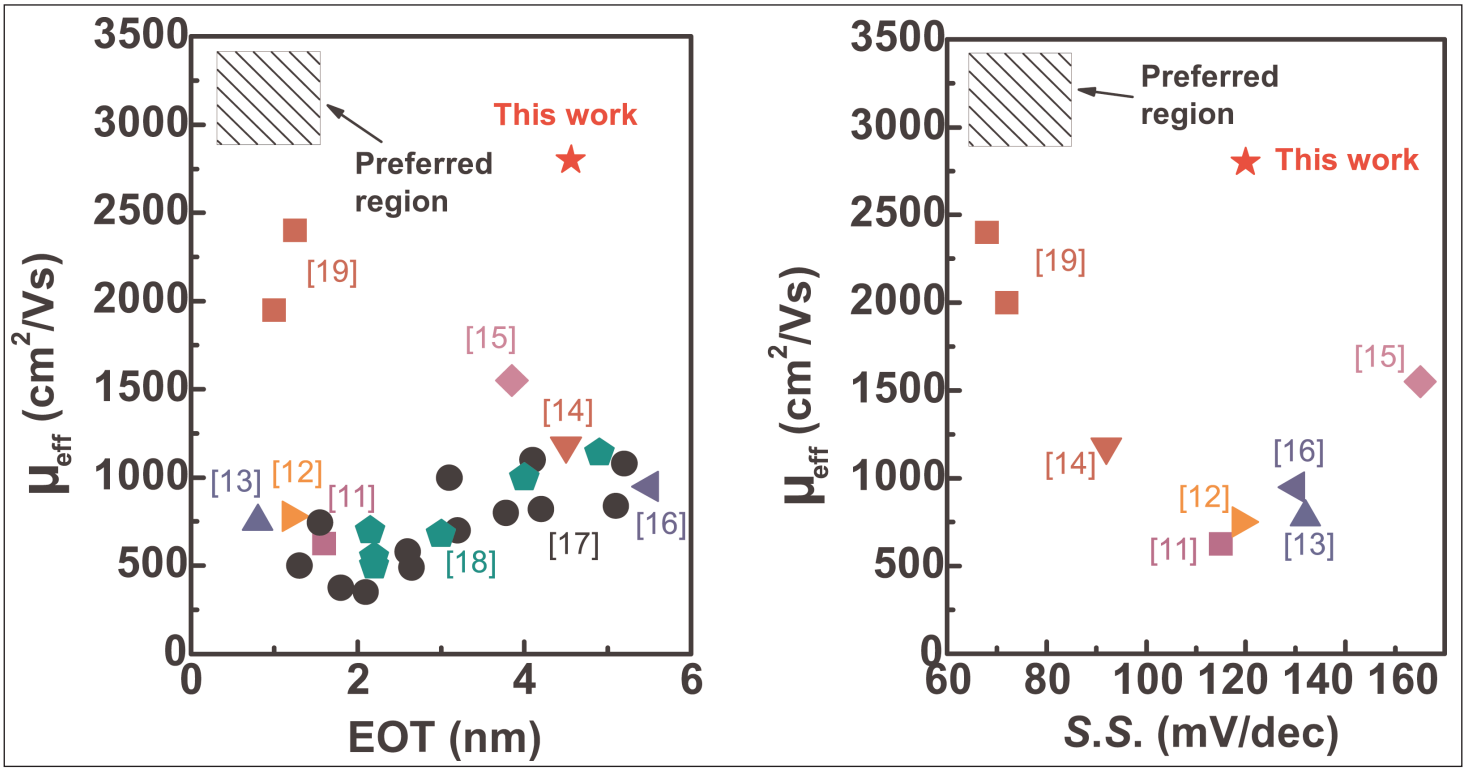

Figure 3. Benchmarks of effective mobility as function of EOT/CET (left) and SS (right) for surface channel InGaAs MOSFETs at 3x10^{12}/cm^2 sheet carrier density.

can be improved from the present thick 10nm/5nm Y_2O_3/Al_2O_3 gate insulator and unoptimized processes. The team comments: "These results highlight the first successful operation of InGaAs-OI MOSFETs fabricated by DWB and ELO." The peak effective channel mobility was 2800cm^2/V-s, claimed as a record high for given equivalent oxide thickness and SS (Figure 3).

The team also demonstrated re-usability of the InP donor wafer, creating transistors with similar performance as those produced from InGaAs layers grown on virgin wafers.

Massachusetts Institute of Technology claimed record self-aligned InGaAs MOSFET performance through mitigation of an anomalous instability mechanism [session 3.4]. According to the team, the anomalous instability arises from electric-field-induced fluorine (F) ion migration and passivation/depassivation of silicon dopants in n-InAlAs cap layers.

The researchers studied devices grown by MBE on InP. Finding that F reactive ion etch of n-InAlAs caused the anomalous instability, the researchers eliminated this material from the part of the structure subjected

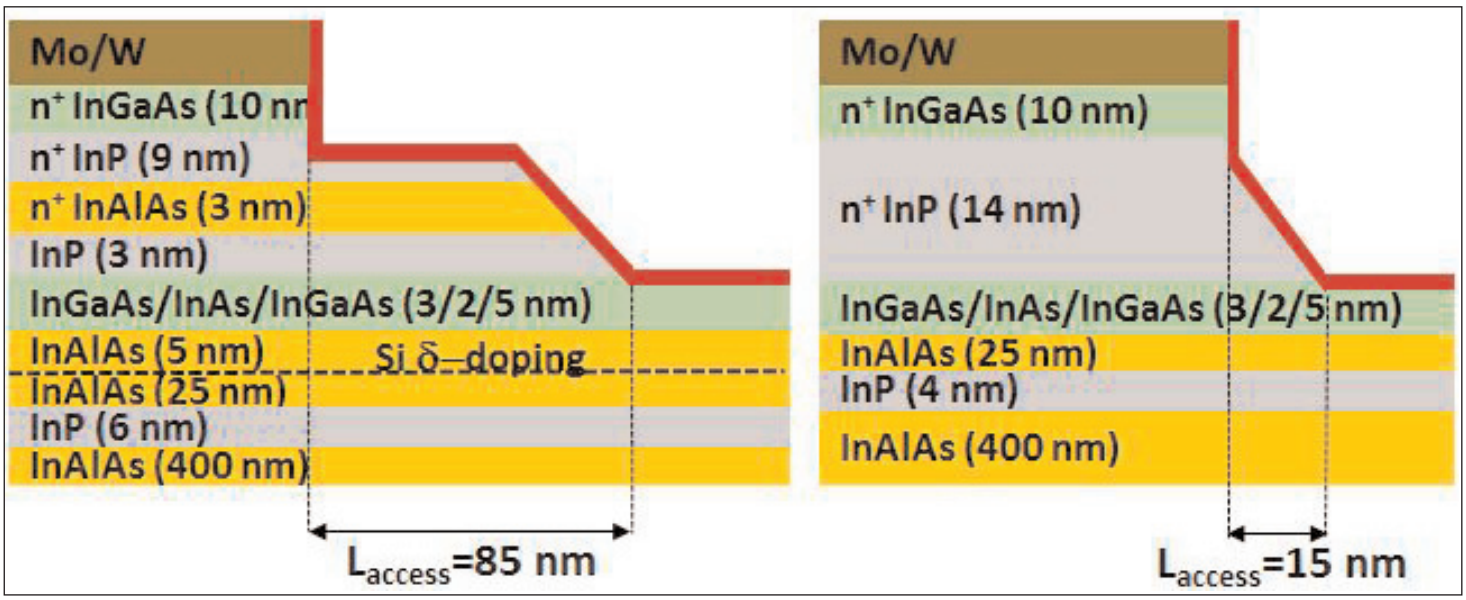

Figure 4. Conventional (left) and alternative (right) device structure with n-InAlAs layer removed to avoid anomalous instability.

to etching, using n-InP instead (Figure 4). The higher electron concentration in the access region of a 70nm-gate-length transistor enabled record low on-resistance of 190Ω-μm and transconductance of 3.45mS/μm, "the highest among InGaAs FETs of any kind," according to the team. The researchers add: "More significantly, the new device structure is far more stable."

Table 1. HRL's mm-wave T-Gate GaN MMIC nodes

Quantities	T2	T3	T4A
Gate length	150nm	40nm	20nm
f_T	90GHz	200GHz	329GHz
f_{max}	220GHz	400GHz	558GHz
Breakdown	> 40V	> 40V	17V
Minimum noise figure at 50GHz	2dB	1.2dB	0.8dB
	SOA prior to NEXT	Advances under NEXT	

The new structure gives a classic positive-bias temperature instability (PBTI) that can be explained as being due to electron trapping in the gate oxide.

A multi-national team reported on record minimum switching slope p-type TFETs using III–V and compound semiconductor heterostructures [session 19.6]. The team was variously associated with Pennsylvania State University, University of Notre Dame, Massachusetts Institute of Technology, Peter Grünberg Institute (PGI-9) and JARA-FIT, Forschungszentrum Jülich GmbH, IMEC, Kurt J. Lesker Company, and Taiwan Semiconductor Manufacturing Company (TSMC).

The III–V structure used p-type $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ tunnel junctions. The group IV devices used a germanium tin ($Ge/Ge_{0.93}Sn_{0.07}$) structure. The gate oxide was applied to the $GaAs_{0.4}Sb_{0.6}$ and $Ge_{0.93}Sn_{0.07}$ parts of the TFETs. The researchers claim that the thinnest gate insulators demonstrate equivalent oxide thickness of ~0.8nm.

The group IV devices exhibited 10x lower interface trap density (D_{it}) compared with the group III–V PTFETs, This enabled the group IV PTFETs to achieve high I_{on} and SS below the planar limit of 60mV/decade at 0.5V drain bias.

GaN/SiC transistors

HRL Laboratories LLC reported on its work developing highly scaled GaN HEMTs and their incorporation into process flows for monolithic microwave integrated circuits (MMICs) [session 3,3]. HRL GaN HEMTs have reached state-of-the-art (SOA) cut-off (f_T) and maximum oscillation (f_{max}) frequencies exceeding 400GHz and 500GHz, respectively. HRL claims that its highly scaled GaN devices have five times higher breakdown voltage than transistors with similar high-frequency RF power gain in other semiconductor systems (Si, SiGe, InP, GaAs).

First-generation MMIC power amplifiers (PAs) achieved power-added efficiency (PAE) of 59% measured at 32GHz frequency with 3V bias and 24.3dBm output power. The researchers claim 15% higher PAE than the best reported for Ka-band (26.5–40GHz) MMICs, along with output power comparable to similarly sized GaAs pseudomorphic and metamorphic HEMT MMICs operating in the 2–3V range.

The researchers believe that their highly scaled GaN transistors could be "excellent candidates for MMIC PAs for next-generation 28GHz, 39GHz, and higher-frequency 5G mobile bands, because they would greatly extend battery lifetime in mobile handsets, due to their superior PAE compared to competing semiconductor technologies."

HRL Laboratories has been working in part under the Nitride Electronic NeXt-Generation Technology (NEXT) Defense Advanced Research Projects Agency (DARPA) program. The MMICs were developed based on HRL's latest T4A HEMT (Table 1) with reduced gate length of 20nm, boosting f_T and f_{max}.

The MMIC process features microstrip and grounded coplanar waveguide (GCPW) interconnects, backside vias, 50Ω/square epi resistors, two metal layers with benzocyclobutene (BCB) interlayer interconnect dielectric with air-box shielding around active devices and SiN_x capacitors.

The Ka-band PA reported at IEDM builds on work reported earlier in the year with low-noise amplifiers (LNAs).

University of California Santa Barbara (UCSB) claimed a record PAE of 27.8% for W-band (75–110GHz) N-polar GaN MISHEMTs [session 3.5]. The device was designed to mitigate dispersion. The associated output power density was 3.0W/mm and the peak gain was 7.4dB at 94GHz.

Panasonic Corp used GaN to create normally-off vertical transistors on GaN substrates with low specific on-state resistance of 1.0mΩ-cm^2 and high breakdown voltage of 1.7kV [session 10.1]. "The vertical GaN transistor with p-GaN/AlGaN/GaN semi-polar gate structure exhibits high threshold voltage of +2.5V and stable switching operation of 400V/15A," the team reports.

The devices (Figure 5) featured a V-groove between the two source electrodes with re-grown undoped GaN and AlGaN layers and p-GaN gate. The initial epitaxial structure included a p-GaN well and a carbon-doped semi-insulating GaN layer. The carbon-doped layer formed a hybrid blocking layer with the p-GaN gate structure, reducing punch-through/off-current leakage. The use of the groove avoided the creation of large electric fields from charge polarization effects that

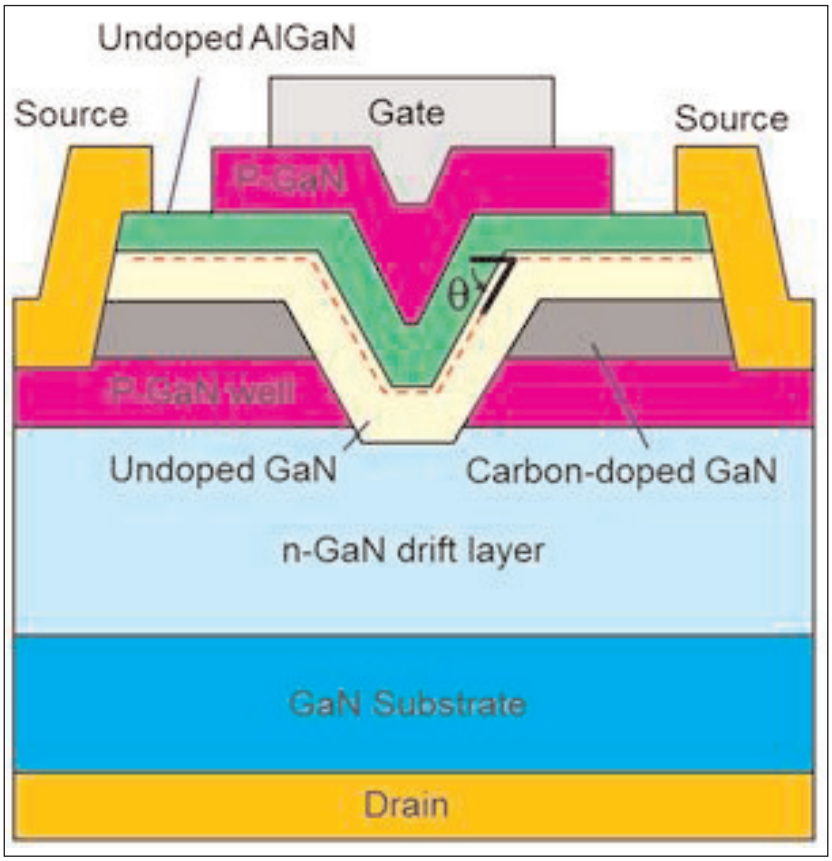

Figure 5. Schematic of vertical GaN transistor with p-GaN/AlGaN/GaN semipolar gate structure.

occur in normal c-plane material. This reduced the sheet carrier concentration of the 2DEG at the AlGaN/GaN interface, increasing the threshold voltage in a positive direction, giving true normally-off behavior.

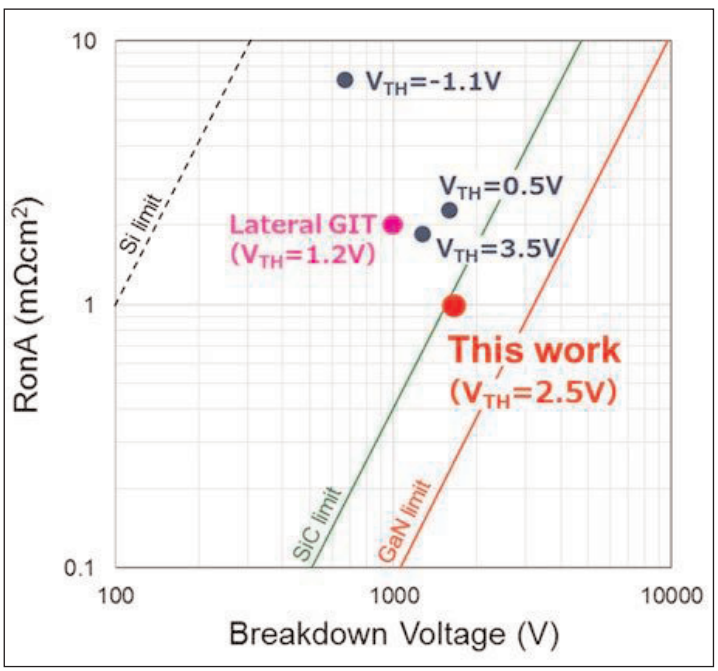

Figure 6. Specific on-resistance (R_{on} x Area) and breakdown voltage of vertical GaN transistor, compared with lateral p-type gate and state-of-the-art GaN-based vertical transistors.

The epitaxial growth and re-growth were achieved by MOCVD. The metalization consisted of titanium/aluminium (Ti/Al) source, palladium/gold (Pd/Au) gate, and Ti/Al/Ti/Au drain. The drain electrode was deposited on the back of the GaN substrate to give a vertical conduction structure.

The device beat the theoretical limit for silicon carbide transistors in terms of on-resistance and breakdown voltage trade-offs (Figure 6). The Panasonic transistor also showed good stability during off-state bias stress tests at 400V drain and 125ºC temperature. The researchers report: "The off-state leakage current and threshold voltage is stable over 300 hours at present indicating further no-change after extension of the testing period. To the best of authors' knowledge, this is the first demonstration of the stable gate performance in vertical GaN transistors."

Massachusetts Institute of Technology, Singapore–MIT Alliance for Research Technology and IQE RF LLC reported on vertical GaN Schottky rectifiers, claiming "greatly enhanced reverse characteristics (10^4-fold lower leakage and 700V breakdown voltage) while maintaining a good forward conduction, with high-temperature (250ºC) operation and fast switching capability" [session 10.2].

The devices (Figure 7) consisted of trenches with corners rounded by a special tetramethylammonium hydroxide (TMAH) treatment to reduce electric field crowding, avoiding premature breakdown. Field rings were formed below the trench bottom with argon ion implantation. The field rings were designed to further

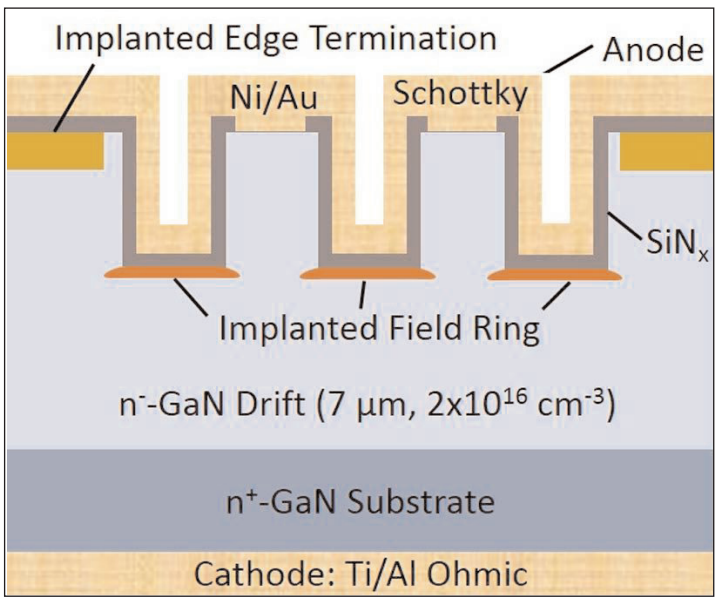

Figure 7. Schematic of developed GaN vertical trench MIS barrier Schottky rectifier with implanted trench rings. Trench depth is 2µm.

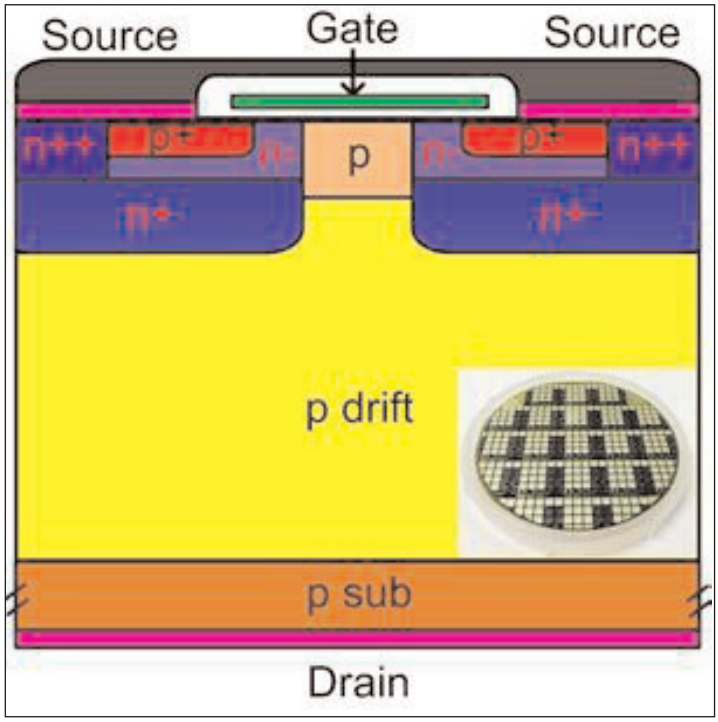

Figure 8. Schematic cross-section and wafer of fabricated SiC p-MOSFET.

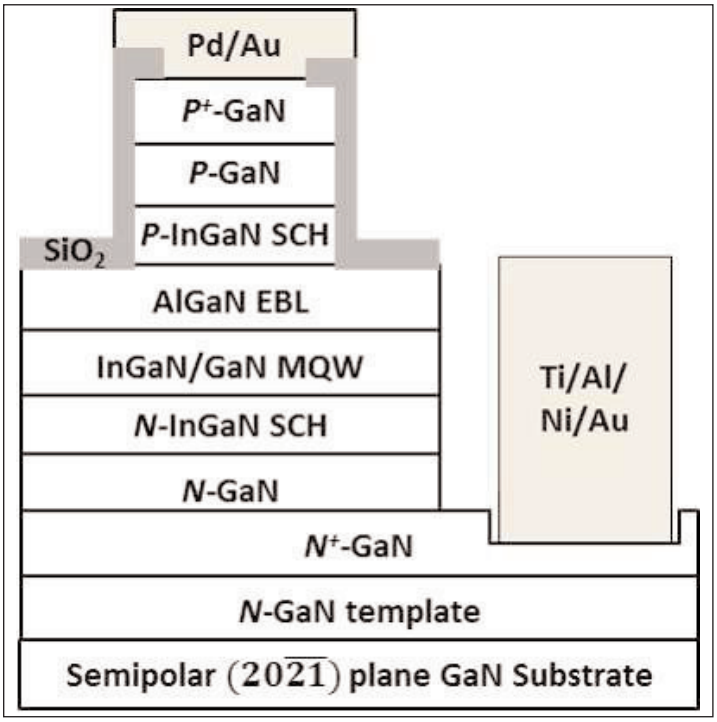

Figure 9. Cross-section of the semiconductor optical amplifier laser diode (SOA-LD) structure.

smooth the electric field stress. The next process step was plasma enhanced chemical vapor deposition of SiN_x. The SiN_x at the top of the trench structure was removed and Ni/Au/Ni was deposited as Schottky contact. The other ohmic diode contact was formed on the back-side of the GaN substrate by annealed Ti/Al.

The researchers claim the devices exhibit the second best on-resistance versus breakdown trade-off, with a high on/off ratio of 10^6 at 600V. The team also reports operation above 200ºC for the first time in a high-voltage GaN vertical Schottky barrier diode.

University of Tsukuba claims the first p-channel vertical 4H-SiC MOSFET fabrication. The breakdown voltage was more than 730V [session 10.7]. At the same time, short-circuit handling was 15% better than that of 4H-SiC n-channel MOSFETs. The researchers suggest applications could include high-frequency complementary inverters.

The MOSFET had a vertical structure based on the n-channel implantation and epitaxial devices (IEMOSFETs) developed by Japan's National Institute of Advanced Industrial Science and Technology (Figure 8). The substrate was Si-face p-type 4H SiC.

The highly doped ($4x10^{18}/cm^2$) n^+-type regions of the bottom part of the channel were formed with nitrogen ion implantation. The lightly doped ($5x10^{15}/cm^3$) n-type material was achieved using epitaxial growth of a 0.5μm layer. The p-type region of the junction FET was provided with aluminium ion implantation.

The gate oxide was a 50nm layer, followed by an annealed polysilicon gate electrode. The 3mmx3mm die was completed with metal deposition of source and drain contacts.

Although the on-resistance of the device is ten times higher than equivalent n-channel devices, the researchers suggest that "this could be greatly improved by adopting advanced cell design, such as super-junction, the trench gate structure and state-of-the-art fabrication technologies."

Optoelectronics

King Abdullah University of Science and Technology, University of California Santa Barbara, and the King Abdulaziz City for Science and Technology have claimed the first experimental demonstration of a two-section semi-polar InGaN-based laser diode with monolithically integrated semiconductor optical amplifier (SOA-LD) [session 22.4].

The SOA-LD material (Figure 9) was grown on semi-polar (20$\bar{2}\bar{1}$) GaN using MOCVD. The device fabrication resulted in 300μm-long SOA and 1190μm-long laser diode sections (Figure 10). The quantum well active region was shared between the sections. The ridge waveguide was 2μm wide. Electrical isolation between the sections was achieved by trench etching and was aided by the high lateral resistance of the InGaN waveguide layer.

With the SOA unbiased (0V), the current threshold for lasing was 229mA. At 250mA the output power was 8.2mW. Biasing the SOA reduced the threshold current and increased output power. At 6V SOA bias, the threshold was 138mA and the output power 28.0mW at 250mA. The 6V SOA bias gives a gain of 5.32dB in output power. The wavelength of the emissions was

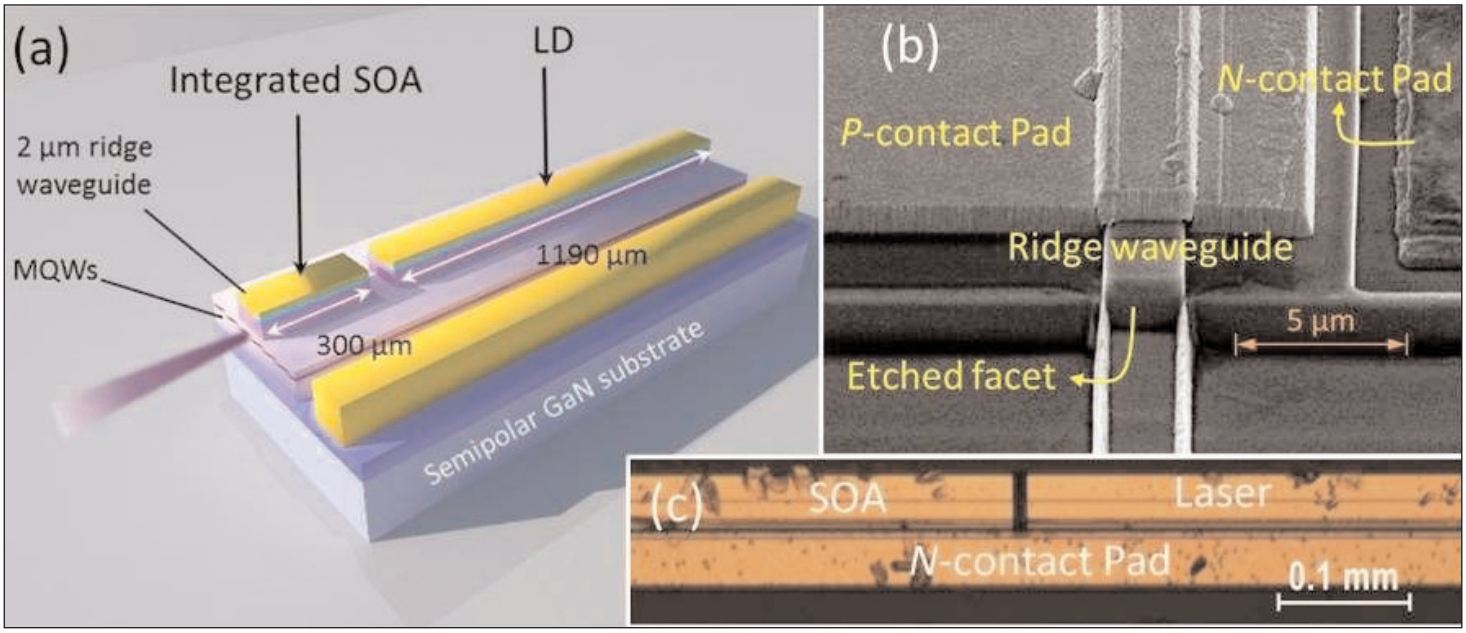

Figure 10. (a) 3D illustration of integrated SOA-LD, (b) elevation-view scanning electron microscope (SEM) image showing the facet and (c) top-view optical microscope image.

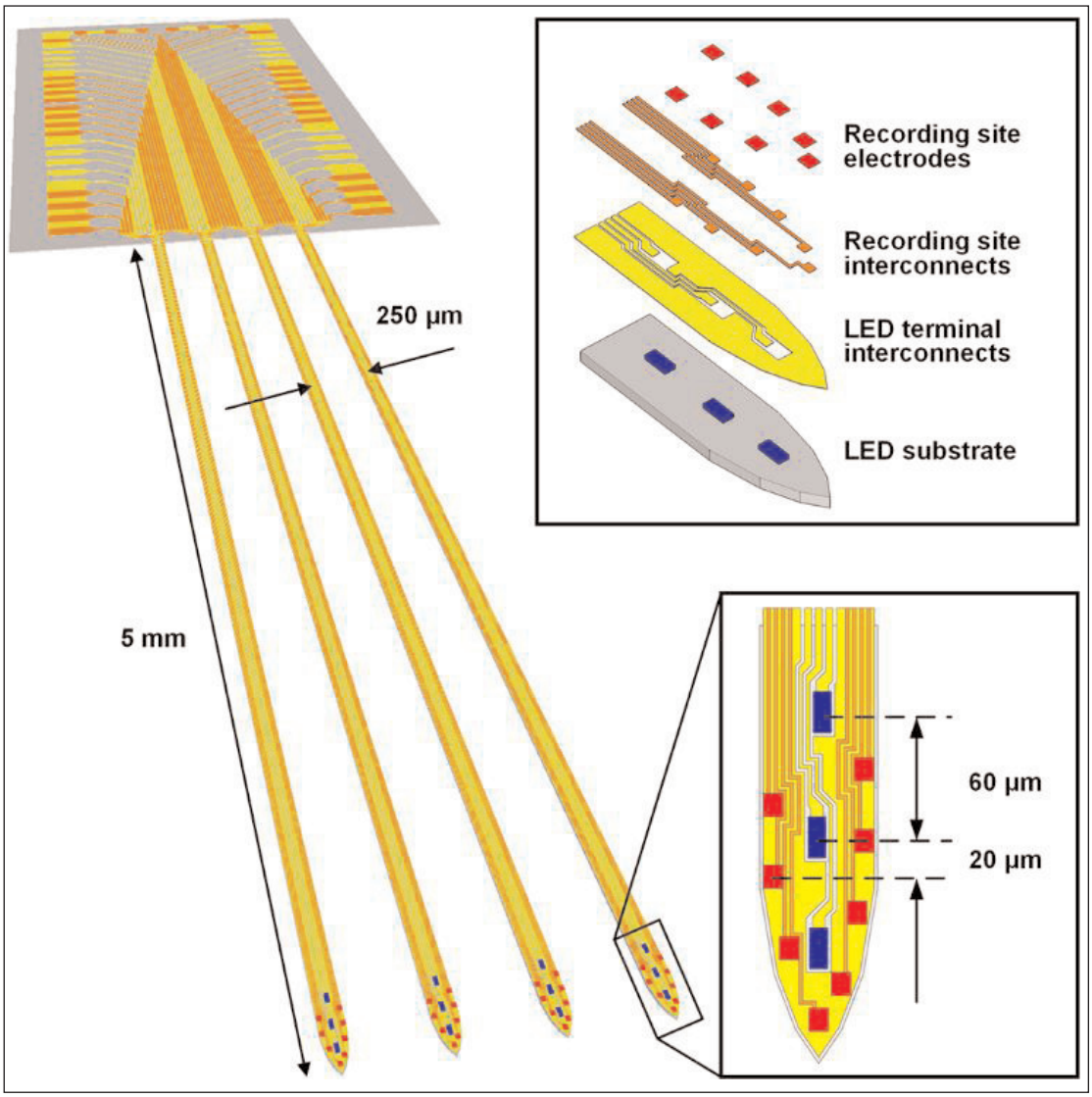

Figure 11. Schematic of GaN-on-Si µLED optoelectrode for high-spatiotemporal-resolution optogenetics. Insets (top right) exploded schematic of optoelectrode tip and (bottom right) top view of optoelectrode tip.

around 404nm.

The researchers also confirmed that the SOA was not acting as an independent laser. No laser emissions were seen up to 71mA — a density of 11.8kA/cm^3. The 138mA threshold of the laser diode section with 6V SOA bias corresponded to a density of 5.8kA/cm^2.

The researchers comment: "The SOA-LD, in the violet–blue–green spectrum range, enables high-power operation of the laser by extending the thermal roll-over to a significantly higher output power, and is promising for applications in visible-light communications, optical interconnects and photonics integrated circuits."

The team foresees solid-state lighting, optical storage, display, optical clocking, and sensing applications. Although these aspects are already covered to some extent by existing laser diodes, an integrated SOA would

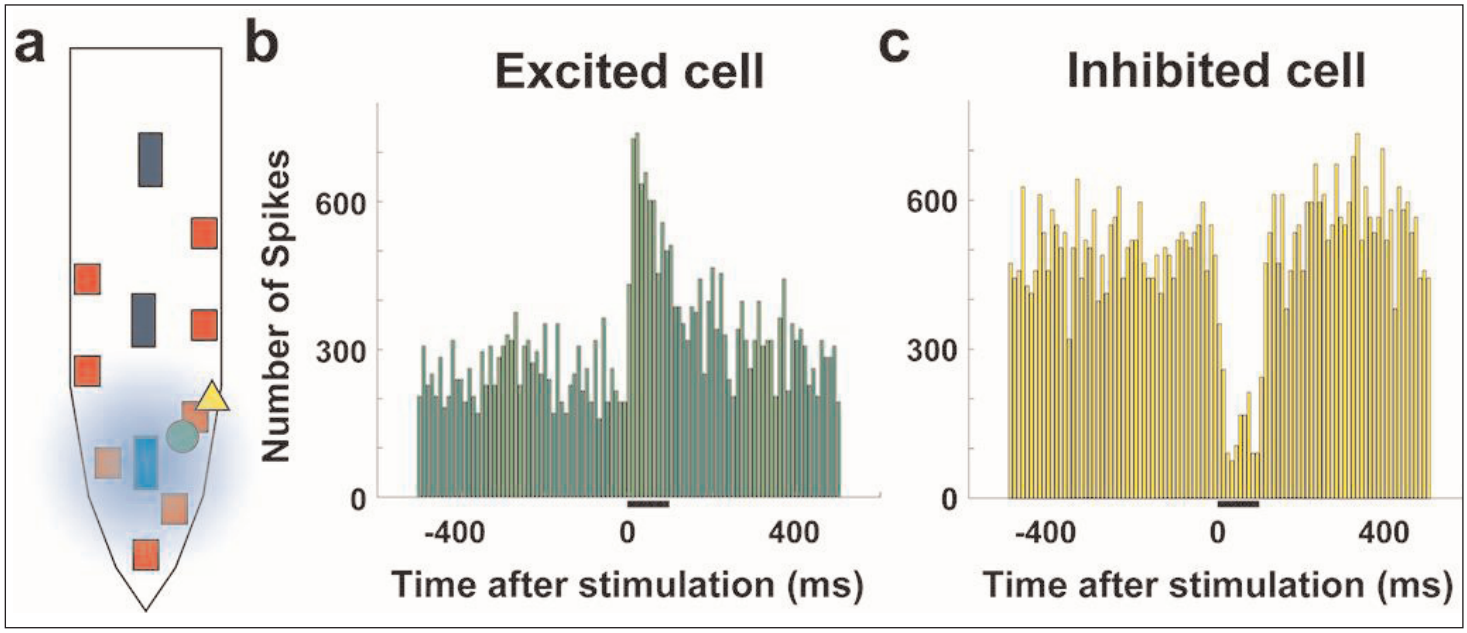

Figure 12. In-vivo validation of light-induced neuronal modulation. (a) Locations of the interneuron (green circle) and the pyramidal neuron (yellow triangle) are identified for monitoring while optically stimulated by the bottommost μLED. (b) Peristimulus time histogram (PSTH) of optically activated interneuron (green circle). (c) PSTH of inhibited non-opsin expressing neuron (yellow triangle) which indirectly responds to optically activated interneuron.

provide space- and power-efficient volume-manufactured components for high-capacity optical communications and high-power pulse generation.

University of Michigan and New York University reported on micro-machined GaN-on-Si μLED optoelectrodes designed for optical stimulation and electrical recording in the brains of genetically modified animals [session 26.5].

The optoelectrode consisted of four 5mmx70μmx30μm shanks (Figure 11). The shanks contained three 15μmx10μm GaN/InGaN μLEDs with 60μm pitch. The shanks also featured eight platinum/iridium site recording electrodes on their tips with 20μm pitch. The conducting interconnections consisted of two metal layers designed to suppress stimulation artifacts that arise from the n-GaN not giving a stable ground potential and thus affecting neighboring devices.

The team foresees solid-state lighting, optical storage, display, optical clocking, and sensing applications. Although these aspects are already covered to some extent by existing laser diodes, an integrated semiconductor optical amplifier would provide space- and power-efficient volume-manufactured components for high-capacity optical communications and high power pulse generation

The epitaxial material for the probes was MOCVD GaN/InGaN multi-quantum well structures on silicon supplied by NovaGaN. Following μLED and electrode fabrication, the optoelectrodes were sculpted by deep reactive ion etch bulk micro-machining. The optoelectrodes were then mounted on four-layer printed circuit boards.

The researchers report: "The measured optical output power suggests that, with as little as 13.8μA of injected current at 3.2V, the μLED is capable of providing 1mW/mm^2, which is the threshold irradiance for activation of channelrhodopsin-2 (ChR2) in neurons at the surface of μLEDs. At 4V, 1.9μW of optical power can be generated, which is equivalent to 12.7mW/mm^2 of radiant flux density at the surface of the μLED and is sufficient to stimulate neurons in more than the adequate volume around the μLED. The peak plug efficiency of the μLED was measured as 0.59±0.07%."

The in-vivo performance of the optoelectrode was tested by implantation in the hippocampal CA1 layer of a freely moving PV-ChR2 transgenic mouse (Figure 12).

STMicroelectronics, CEA-LETI, Vistec Electron Beam GmbH, and University of Grenoble Alpes claimed the first integration of a III–V/Si hybrid laser on the backside of a SOI wafer [session 22.2]. The aim was to preserve compatibility with Si-waveguide integration and with CMOS front-side metal interconnects, allowing passive and active photonic device integration. ■

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.