High-mobility AlGaN/GaN heterostructures grown on silicon substrates using simple stress control technique

Peking University researchers have recently increased mobility to 2240cm^2/Vs at sheet charge density of 7.7x10^{12}cm^{-2} for AlGaN/GaN heterostructures grown on silicon substrates using a low-aluminium-content AlGaN buffer layer.

Researchers in Peking University of China (PKU) have demonstrated high-quality AlGaN/GaN heterostructures grown on silicon substrates using a simple stress control technology with a low-aluminium-content AlGaN layer. [J. P. Cheng et al, Appl. Phys. Lett. 106, 142106 (2015)]. The use of this technology allows for high-mobility AlGaN/GaN heterostructures with electron mobility of 2040cm^2/Vs at sheet charge density of 8.4x10^{12}cm^{-2}. Very recently, by further balancing the stress and optimizing the growth conditions, the mobility has been improved to 2240cm^2/Vs at sheet charge density of 7.7x10^{12}cm^{-2}.

The researchers comment: "Thanks to the simple AlGaN buffer layer, this is a cost-effective method for realizing crack-free AlGaN/GaN heterostructures grown on Si substrates while maintaining high material quality."

For AlGaN/GaN HEMT on silicon substrate, the material quality and reliability, which are supposed to be related to dislocation density, remains a challenge to their widespread use. To date, there has not been much success in achieving high-quality AlGaN/GaN heterostructures grown on silicon substrates with two-dimensional electron gas (2DEG) mobility larger than 2000cm^2/Vs, even although such high values

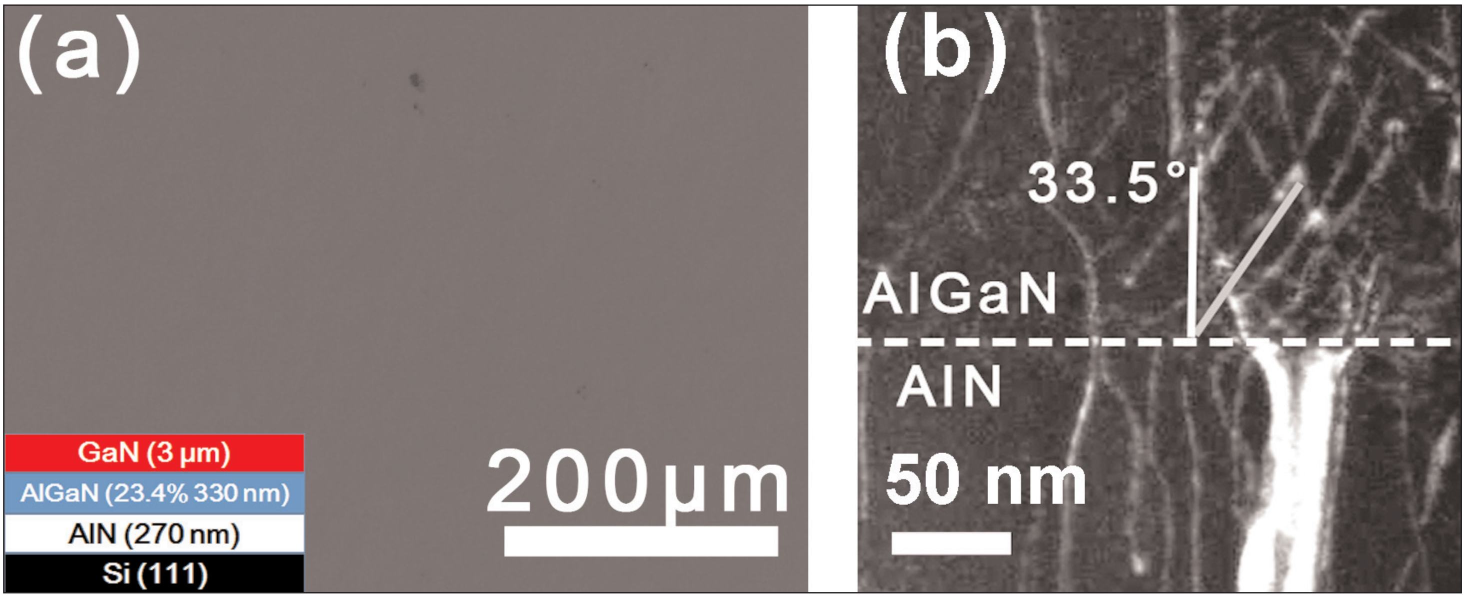

Figure 1. (a) Optical images of the sample. The insets show the corresponding cross-sectional diagrams for the sample. (b) Weak-beam g = (11$\bar{2}$0) TEM images of the samples. The average bend angle of dislocation inclination at the top of AlN buffer layer is about 33.5°.

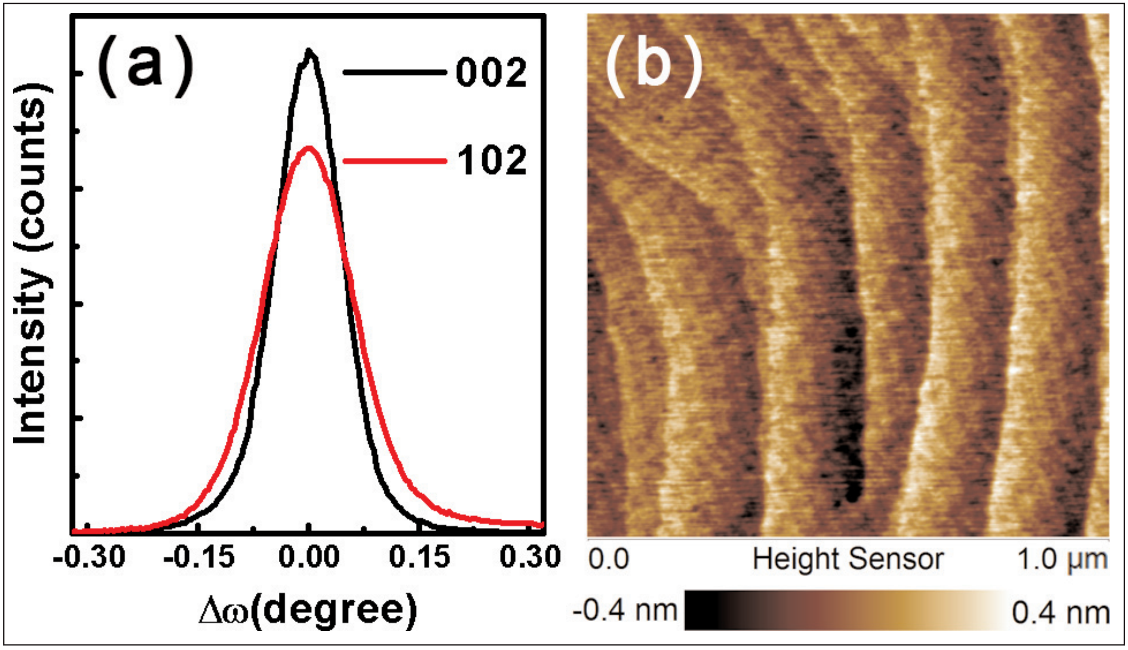

Figure 2. (a) Symmetric (002) and asymmetric (102) ω-scans of rocking curve in GaN layer of the sample. (b) AFM image.

have been reported for similar structures grown on silicon carbide (SiC) or sapphire substrates. The main reason is that the dislocation density in GaN layers is still higher than that grown on SiC or sapphire substrates. Also, regarding mass production. the complicated buffer layers that are generally used suffer from a time-consuming growth process. In order to solve these issues, it is necessary to develop a cost-effective GaN-on-Si technology to further reduce the dislocation density.

The PKU team has hence developed a simple stress control technology to grow a high-quality GaN layer on silicon substrates. The GaN layers were grown on 4-inch p-type Si (111) substrates by metal-organic chemical vapor deposition (MOCVD). The sample structure (inset of Figure 1(a)) consisted of a 270nm AlN layer, a 330nm $Al_{0.23}Ga_{0.77}N$ buffer layer, and a 3µm GaN layer.

The material surface is crack free (Figure 1(a)). The average bend angle of dislocation inclination at the top of the AlN buffer layer is about 33.5°, as shown in the TEM image (Figure 1(b)). "The inclination of the dislocations is associated with the compressive stress induced by the lattice mismatch between the AlN and AlGaN layers," comment the researchers. "The large bend angles enhance the probability for dislocations to encounter and react with other ones," they add. "Upon entering the GaN layer, the dislocation density is reduced and then less compressive stress is consumed during dislocation evolution. As a result, more residual compressive stress is thus left to compensate the thermal tensile stress. This technology can filter dislocations and further reduce dislocation density, especially the edge dislocation density, which is essential to maintain the higher compressive stress."

The FWHM of the GaN (002) and (102) rocking curves for the sample are 389 arcsec and 527 arcsec, respectively (Figure 2 (a)). The corresponding AFM image (Figure 2(b)) presents atomic-step terraces. The root mean square (RMS) roughness is 0.11nm in a scanned area of 1µm x 1µm. These indicate that a high-quality

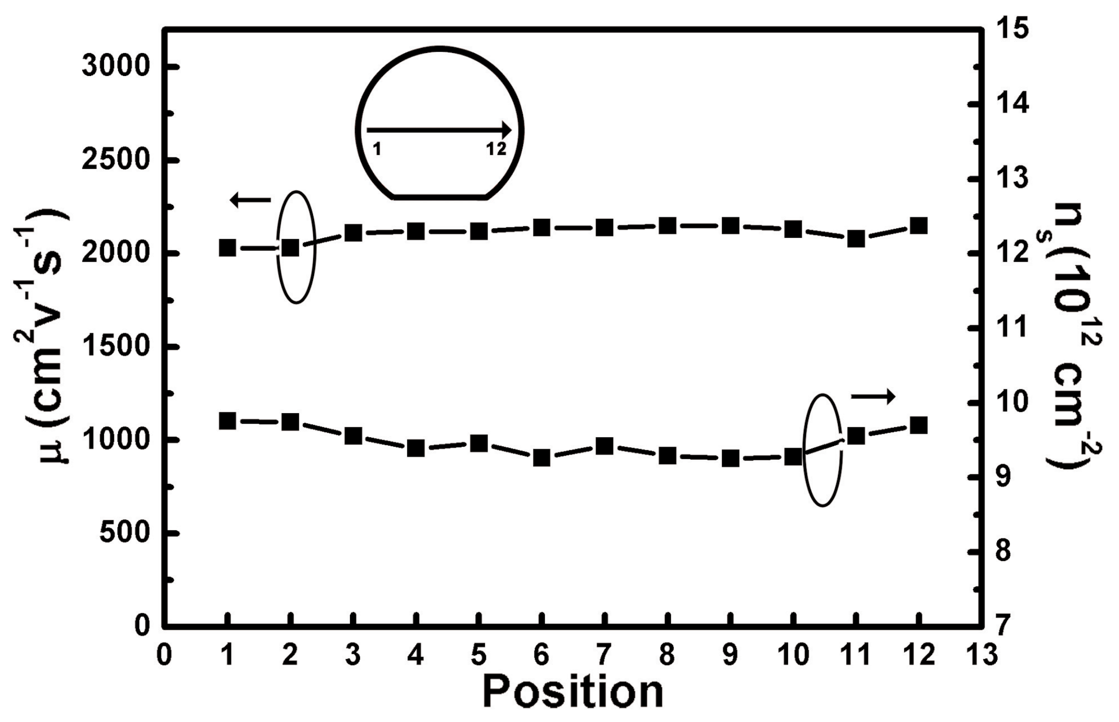

Fig. 3 The 2DEG density and mobility distribution across the AlGaN/GaN heterostructure sample. The inset shows the measured positions on the wafer.

and crack-free 3μm-thick GaN layer has been grown on a silicon substrate using this low-Al-content AlGaN intermediate layer.

Using this high-quality and crack-free GaN layer as the buffer layer, the researchers fabricated an $Al_{0.20}Ga_{0.80}N$ (~22nm)/AlN (~1nm)/GaN heterostructure. Room temperature Hall measurements using the Van der Pauw configuration on mesas with a 5cm x 5cm geometry showed that the 2DEG mobility and carrier density were 2040cm^2/Vs and 8.4x10^{12}cm^{-2}, respectively. The corresponding sheet resistance is about 367Ω/sq. Recently, the results have been improved by further balancing the stress and optimizing the growth conditions. The AlGaN/GaN heterostructures are very uniform, with a maximum electron mobility of 2150cm^2/Vs at an electron density of 9.3x10^{12}cm^{-2} (Figure 3). The sheet resistance across the wafer is as low as 313 ± 4Ω/sq, and hence the uniformity value is only 1.3%. For some wafers with a slightly lower-Al-content AlGaN barrier layer, the maximum electron mobility can be up to 2240cm^2/Vs at sheet charge density of 7.7x10^{12}cm^{-2}. The results are among the best reported in the literature for AlGaN/GaN heterostructures grown on silicon substrates, according to the researchers. They also fabricated AlGaN/GaN HEMTs with a gate-to-source distance, gate-to-drain distance and gate length of $L_{GS}/L_{GD}/L_G$ = 1.5μm/3μm/1.5μm. The initial results show excellent DC characteristics, with a maximum drain current density (I_{Dmax}) of 688mA/mm.

"This stress control technology is efficient for improving the crystal quality," comment the researchers. "Furthermore, the buffer structure with a single low-Al-content AlGaN intermediate layer is simpler than the commonly used complicated buffers and could reduce growth time and thus the cost," they add. "This technology can also be used during growth of InAlN/GaN heterostructures. On the other hand, it is easy to make the low-Al-content AlGaN layer conductive with silicon doping, which demonstrates the potential for fabrication of GaN-on-Si vertical devices. These results look promising for future low-cost and high-performance GaN-on-Si electronic devices." ■

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