# Gallium oxide beats silicon power limit

## Researchers report simultaneous high breakdown/low resistance in $\beta$-$Ga_2O_3$.

Researchers based in the USA claim the first more than 4kV-capable $\beta$-$Ga_2O_3$ lateral metal–semiconductor field-effect transistors (MESFETs) surpassing the theoretical unipolar figures of merit (FOMs) for silicon-based devices [Arkka Bhattacharyya et al, Appl. Phys. Express, v15, p061001, 2022].

The team from University of Utah, University at Buffalo, Agnitron Technology Inc and University of California Santa Barbara (UCSB) also say that, to date, the devices show the highest maximum drain current ($I_{DMAX}$) and lowest on-resistance ($R_{ON}$) simultaneously for any $\beta$-$Ga_2O_3$ with breakdown voltage ($V_{BR}$) more than 4kV.

The 4.6–4.9eV ultra-wide bandgap of $\beta$-$Ga_2O_3$ implies high breakdown capabilities with potential for power-efficient next-generation high-voltage power devices. Breakdown voltages up to 8kV have been achieved, but practical devices also need low resistance for power efficiency.

A 230nm layer of $\beta$-$Ga_2O_3$ was grown on an iron-doped bulk substrate oriented as (010). The researchers used Agnitron's Agilis 700 metal-organic vapor phase epitaxy (MOVPE) equipment with triethyl-gallium and oxygen precursors. Silane ($SiH_4$) was the source for n-type silicon doping.

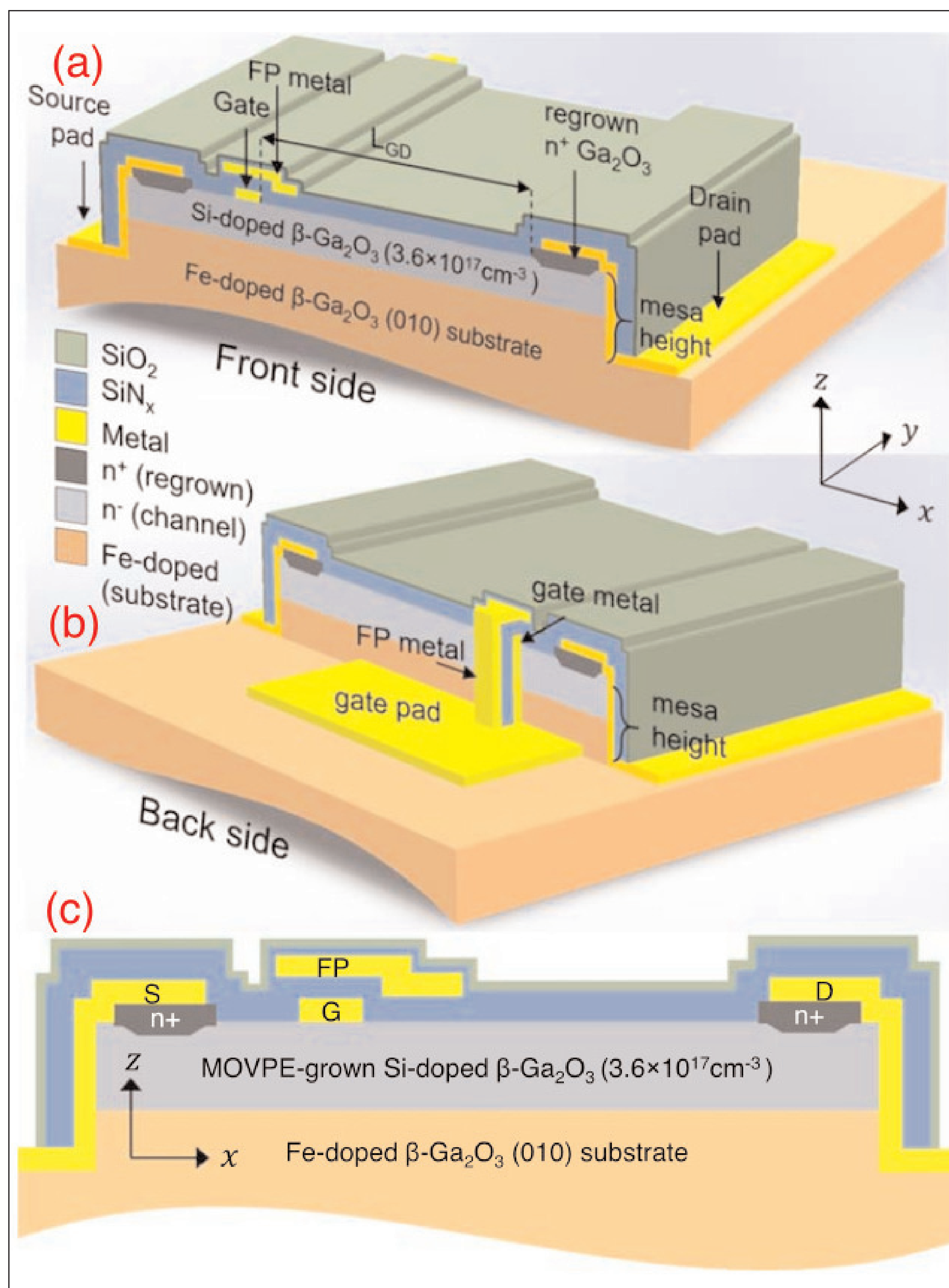


**Figure 1. (a) 3D cross-section schematic of $\beta$-$Ga_2O_3$ MESFET showing FP design. (b) Gate FP metal electrically connected to gate pad outside mesa (inset: coordinate planes/axes) and (c) 2D cross-section schematic along x–z plane.**

The mesa and recessed contact regions were fabricated using sulfur hexafluoride ($SF_6$)/argon inductively coupled plasma reactive ion etch (ICP-RIE) — see Figure 1. The mesa height was 500nm, meaning that the etch continued into the substrate. The ohmic contact region

consisted of heavily doped $n^+$-$\beta$-$Ga_2O_3$ regrown in the recessed region.

The MESFET consisted of annealed titanium/gold/nickel ohmic source/drain contacts and a nickel/gold/nickel Schottky gate.

The titanium/gold/nickel gate field plate (FP) was insulated from the gate metal with 170nm of plasma-enhanced chemical vapor deposition (PECVD) silicon nitride ($SiN_x$). The electrical connection between the gate and FP was made away from the device mesa. The FP fabrication was designed to avoid plasma-related damage in the active region.

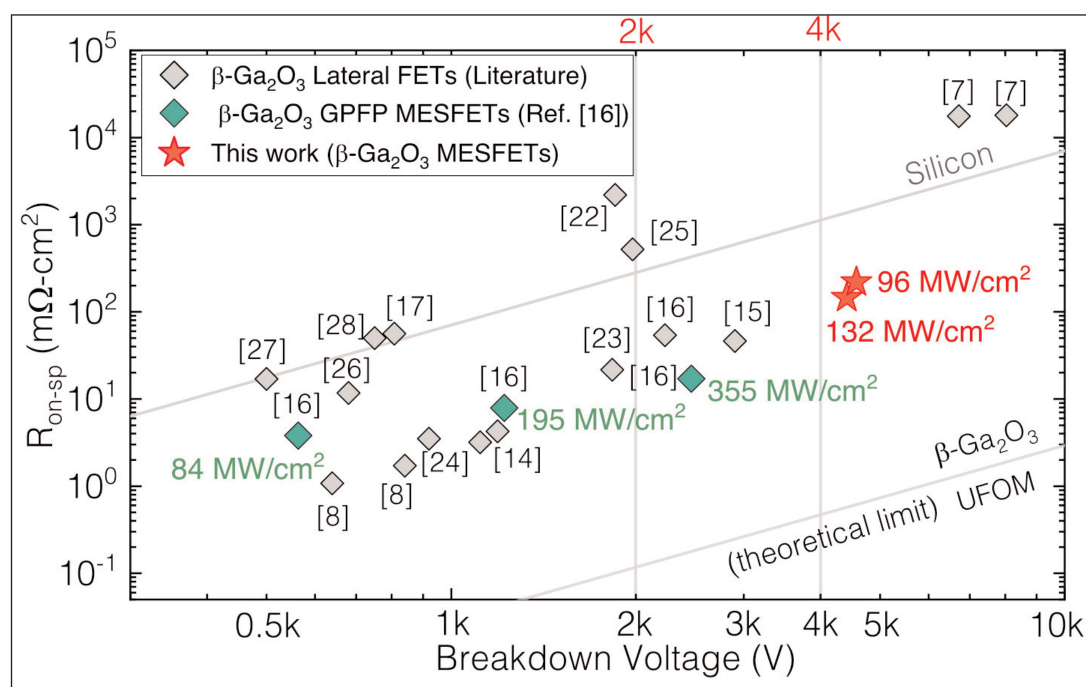


**Figure 2. Differential $R_{on,sp}$–$V_{BR}$ benchmark plot of latest $\beta$-$Ga_2O_3$ MESFET with literature reports. Green data represent previous work of the team.**

The device mesa was finally passivated with a combination of 50nm silicon nitride and 50nm silicon dioxide. The gate length of the devices was 2.4μm, and the gate–source spacing 1μm.

Hall measurements gave a channel charge carrier density and mobility of $5.7x10^{12}m^2$ and $95cm^2$/V-s, respectively. The corresponding sheet resistance was 11.7kΩ/square.

The maximum on-current in devices with 34.5μm gate–drain distance ($L_{GD}$) and 3.2μm FP was 56mA/mm at 2V gate potential. The on-resistance was 385Ω-mm. The device pinched-off sharply with the gate at –13V. The on/off current ratio was more than 108. The maximum transconductance was 6.2mS/mm, and the sub-threshold swing 186mV/decade.

The breakdown characteristics were explored with the devices submerged in FC-40 Fluorinert dielectric liquid. The breakdown voltage, with the device off at –20V gate potential, occurred with a drain-gate potential difference of 4415V. This naturally increased with 44.5μm $L_{GD}$ (3.5μm FP) to 4567V. Before the catastrophic breakdown the leakage varied in the range 10–100nA/mm.

The researchers attribute the improved breakdown performance on steps taken to minimize reverse leakage. The team comments: "The long HF substrate cleaning before the epilayer growth helped in suppressing the parasitic channel at the epilayer/substrate interface that is believed to come from residual silicon impurities from the substrate polishing or ambient exposure." They also believe that the mesa etching deep into the substrate eliminates fringing leakage paths around the device mesa.

Devices with $L_{GD}$ less than 10μm demonstrated average breakdown fields ($V_{BR}/L_{GD}$) around 2.5MV/cm. Above 10μm $L_{GD}$ the $V_{BR}$ tended to saturate around 4.5kV.

On the basis of simulations, the researchers suggest that below 10μm $L_{GD}$ the field profile was of a punchthrough form with non-zero field at the drain contact at breakdown. Longer $L_{GD}$ resulted in a non-punchthrough field up to breakdown.

The simulations also raised concerns of the peak field occurring at the FP edge in the silicon nitride layer: "Dielectric leakage/breakdown could also be limiting the $V_{BR}$ and causing the saturation in $V_{BR}$." The team suggests that the dielectric performance would be improved by using materials with a high product of relative DC dielectric permittivity (ε) and critical electric field for breakdown.

The $V_{BR}^2/R_{on,sp}$ power figure of merit (PFOM) reached $132MW/cm^2$ for 34.5μm $L_{GD}$. The specific on-resistance was normalized according to $L_{GD}$ and the transfer lengths of the source/drain contacts (0.6μm each). The longer 44.5μm $L_{GD}$ resulted in a lower $96MW/cm^2$ PFOM.

Commenting on benchmarking against other reports (Figure 2), the researchers write: "It can be seen that the devices reported here are the first >4kV-class $\beta$-$Ga_2O_3$ FET devices to surpass the theoretical unipolar FOM of silicon. Furthermore, our reported $R_{on,sp}$ are the lowest for any $\beta$-$Ga_2O_3$ FET exceeding a breakdown voltage of 4kV." ■

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