Hybrid III-nitride and silicon carbide high-voltage power transistors

Device simulations suggest proposal could combine high mobility with higher OFF-state voltages.

Researchers at Hong Kong University of Science and Technology (HKUST) are proposing using III-nitride and silicon carbide (SiC) hybrid technologies for high-voltage power devices [Jin Wei et al, IEEE Transactions on Electron Devices, vol63, p2469, 2016].

The researchers are looking to improve on the performance of silicon-based devices by using materials that can sustain higher electric fields before breakdown — a quality associated with wider bandgaps as seen in SiC and aluminium gallium nitride (AlGaN).

SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) can sustain high OFF-state voltages but suffer from low channel mobility. By contrast, AlGaN/GaN high-electron-mobility transistors (HEMTs) have high mobility (as the device name suggests), but suffer from problems with current collapse on switching due to delays from charge trapping. Current collapse would seem to restrict the potential use of lateral AlGaN/GaN HEMTs to applications lower than 1000V. The problem

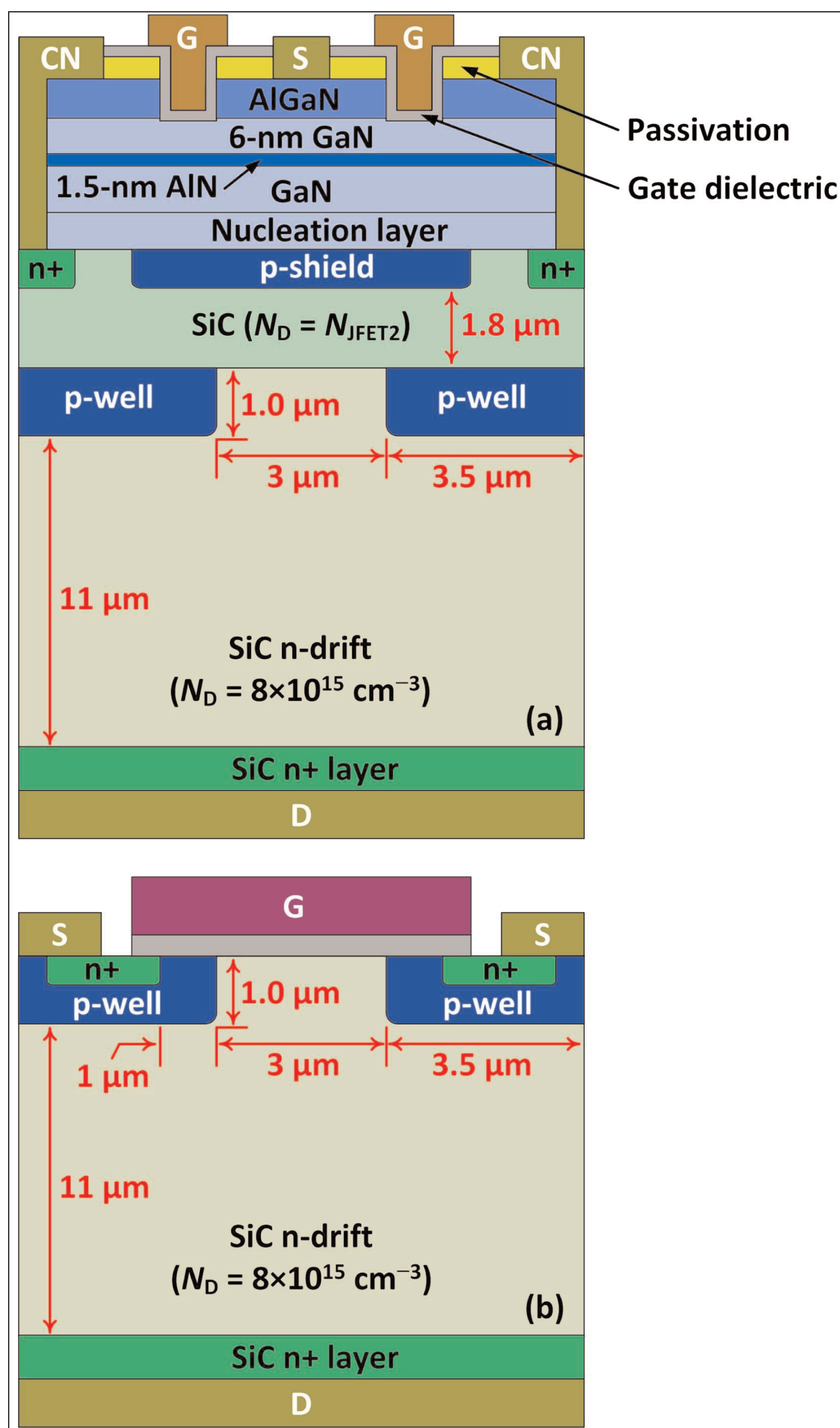

Figure 1. Schematics of (a) proposed GaN/SiC HyFET and (b) conventional SiC MOSFET. HyFET consists of AlGaN/GaN channel and SiC voltage-blocking portions, electrically connected by CN connection contact. Also, p-wells and p-shield in HyFET are connected to source terminal. JFET1 is the region between p-wells. JFET2 is the region between p-shield and p-wells.

could perhaps be solved by adopting a vertical structure, but this would need growth on very expensive GaN substrates. Some first steps have been taken, but an effective implantation technique has yet to be developed for creating p-type wells.

The HKUST research proposes combining III-nitride epitaxial layers on SiC to create hybrid FETs (HyFETs). The team comments: "Since epitaxial growth of GaN layers on SiC substrate is a rather mature technology, a superior power device is expected if the merits of SiC devices and GaN HEMTs are combined on a single platform."

HKUST simulated a device with AlGaN/GaN high-mobility channel and vertical SiC drift region for high OFF-state voltages. In addition to three HKUST researchers (Jin Wei, Qimeng Jiang, Kevin J. Chen), Huaping Jiang of both Dynex Semiconductor Ltd in the UK and Zhuzhou CRRC Times Electric Co Ltd in China contributed to the work.

Dynex develops and markets high-power bipolar discrete semiconductors, along with insulated-gate bipolar transistors (IGBTs), electronic assemblies and components. Zhuzhou CRRC Times Electric is concerned with propulsion and control systems for high-speed trains, electric multiple unit (EMUs), mass transit, and for electric and diesel locomotives.

The proposed structure (Figure 1) uses an AlGaN/GaN channel portion for gate control on a SiC substructure that is designed to maintain a good OFF-state.

The p-type regions of the SiC structure could be achieved using aluminium implantation and activation at 1650°C. The JFET2 region between the p-wells and p-shield would be achieved by epitaxial regrowth. The p-shield depth is 0.2μm.

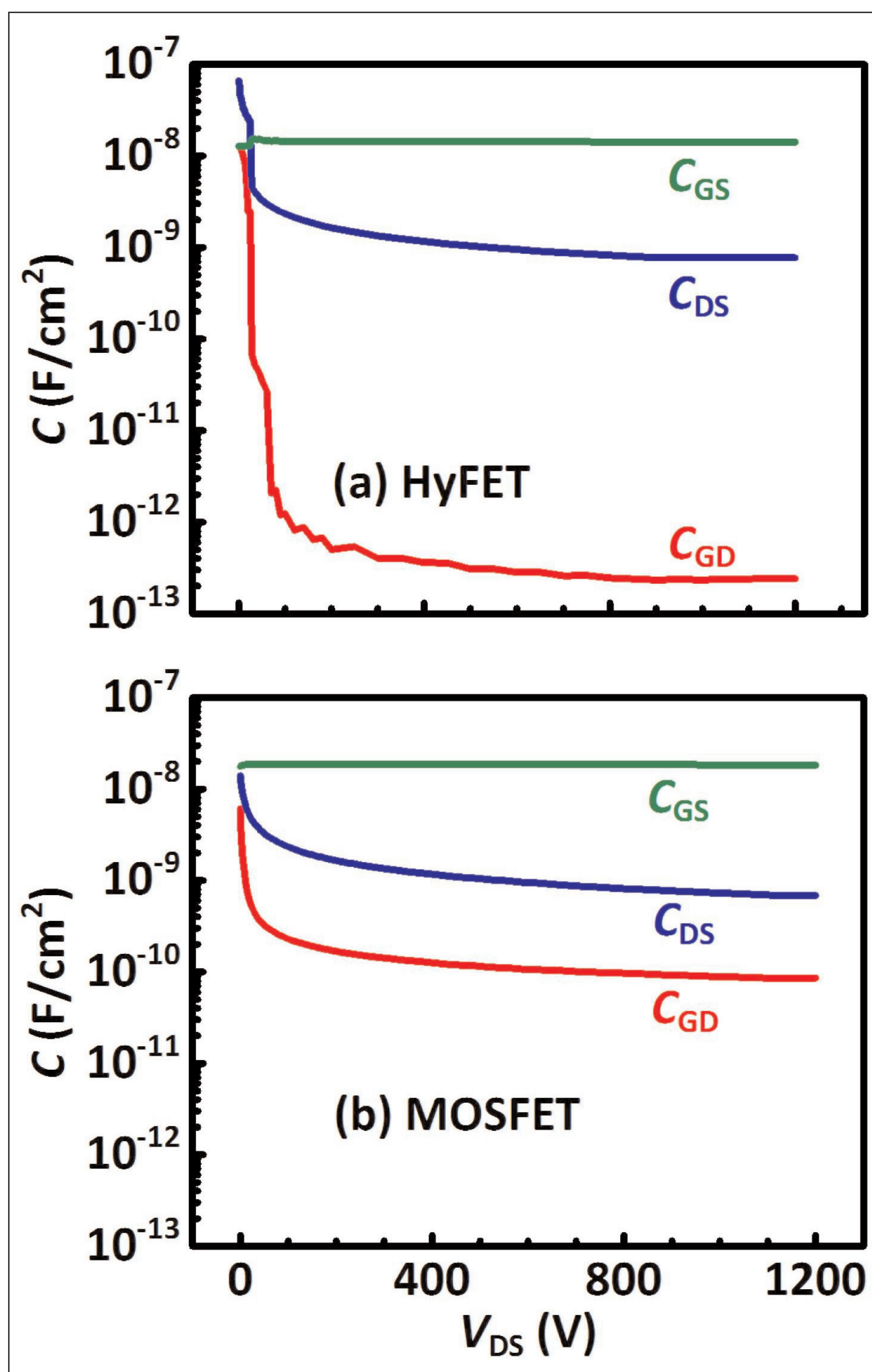

Figure 2. Terminal capacitances of (a) GaN/SiC HyFET and (b) SiC MOSFET.

The AlGaN/GaN region could be grown either by metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). Connections to the n$^+$ (CN) and p-type regions in the SiC substructure could be achieved by dry etch of via holes through the AlGaN/GaN layer.

One aspect that does not seem to be fully developed as yet is a high-temperature anneal for the GaN/SiC contacts. The researchers suggest that this might need a multi-step process.

Although there are a number of techniques in the literature for giving enhancement-mode (normally-off) operation in the AlGaN/GaN structure, the researchers decided to model a relatively new double-channel MOS gate structure that has been demonstrated by HKUST [Jin Wei et al, IEEE Electron Device Letters, vol36, p1287, 2015]. The second channel is created by a 1.5nm AlN insertion layer. The gate recess is terminated by the upper channel at the AlGaN/GaN interface. This maintains a high mobility in the lower AlN/GaN channel by avoiding etch degradation.

One variable in the model, the n-type doping in the JFET2 region (NJFET2), was subject to a delicate compromise between low ON-state resistance and the ability to deplete the region for the OFF-state. The CN voltage used to achieve the OFF-state is higher with high NJFET2, and this can reduce the reliability of the overlying AlGaN/GaN channel. The modeling

suggested that NJFET2 of $5x10^{16}/cm^3$ gave a balance between low ON-resistance and a relatively low OFF CN voltage of ~50V.

The hybrid structure gives a sharper turn-on with gate voltage compared with the SiC MOSFET: at 5V HyFET gate potential the ON resistance was 26mΩ-cm^2, while the MOSFET at 20V gate had 4.6mΩ-cm^2. The main improvement arises due to reduced channel resistance — 52% of the overall value in the MOSFET, compared with 7% for the HyFET, excluding contact and substrate resistances.

The HyFET has a lower OFF-state breakdown voltage of 1581V, compared with 1716V for the MOSFET. This is blamed on "more severe electric field crowding at the corners of the p-wells".

On the other hand, the gate–drain capacitance (C_{GD}) of the HyFET is "dramatically reduced" — by almost three orders of magnitude compared with the MOSFET (Figure 2). "A low C_{GD} is of great importance in reducing the switching loss," the researchers write.

The HyFET setup also reduced gate charge in a simulated test circuit with supply voltage 600V and load current 100A. The circuit included a SiC Schottky barrier diode that provided a freewheeling path. The transistors were $1cm^2$ in area. For the HyFET, the gate charge (Q_G) was found to be $239nC/cm^2$ and the gate–drain charge (Q_{GD}) was $47nC/cm^2$. The corresponding figures for the SiC MOSFET were $885nC/cm^2$ and $223nC/cm^2$. The very low gate–drain charge is related to the improved C_{GD} for the HyFET.

The researchers comment: "Low values of Q_G and Q_{GD} are highly desired for power FETs, since a lower Q_G is beneficial for reducing the driving loss, while a lower Q_{GD} results in a smaller switching loss." ■

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