Boosting transconductance and squeezing off-current

Taiwan's National Yang Ming Chiao Tung University claims transconductance among the highest for InGaAs FinFETs so far.

National Yang Ming Chiao Tung University in Taiwan has reported increased transconductance (g_m) and reduced OFF-current (I_{OFF}) for indium gallium arsenide (InGaAs) fin field-effect transistors (FinFETs) from remote nitrogen plasma passivation of the gate insulation layers [Hua-Lun Ko et al, IEEE Transactions on Electron Devices, volume 69, issue 2 (February 2022), p495].

The devices were fabricated from n^+-InGaAs on heavily p-type indium phosphide (p^+-InP). The source/drain regions were doped with silicon implantation and activation annealing. The fins were etched with plasma, followed by citric acid sidewall smoothing and fin-width shrinking. The fins were oriented in the (010) crystal direction to give the highest aspect ratio.

The gate insulators consisted of 0.8nm aluminium nitride and 2.9nm hafnium dioxide, both applied using atomic layer deposition (5 cycles and 30 cycles, respectively). The insulation was treated with nitrogen (N_2) remote plasma (RP) in-situ to fill oxygen vacancies in the high-k materials. This reduced the OFF-current density in all devices to less than 5×10^{-4}μA/μm. Further, the team comments: "Additionally, trap-assisted tunneling (TAT) and Frenkel–Poole emission are greatly inhibited by N_2 RP passivation."

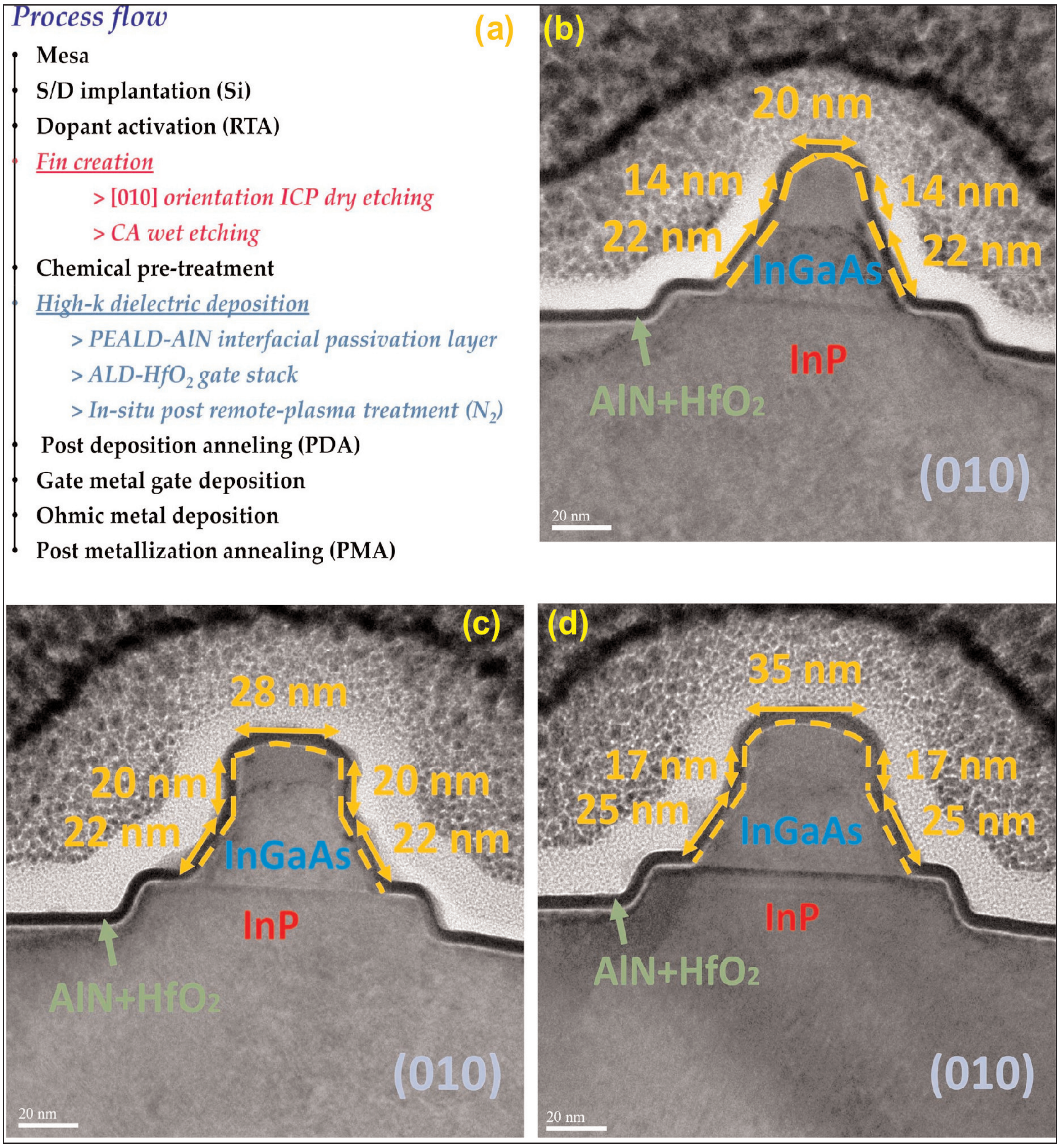

Figure 1. (a) FinFET fabrication. Cross-sectional high-resolution transmission electron microscope images of fins of width 20nm, (c) 28nm and (d) 35nm.

The researchers estimate that the equivalent oxide thickness of these high-k layers is 0.8nm.

The devices were completed by annealing at 450°C in forming gas (hydrogen/nitrogen mix), gate metal deposition, ohmic source/drain metalization, and post-metalization annealing.

The resulting devices demonstrated high ON-current and peak transconductance (Figure 2). "The devices fabricated in this work showed highest g_m of 2727μS/μm, highest I_{ON} of 835μA/μm, high Q-factor ($Q = g_m/SS_{sat}$) of 22.3, high I_{ON}/I_{OFF} current ratio of 3×10^5, and low OFF-current of 4.5×10^{-4}μA/μm for Lch = 45nm and W_{fin} = 35nm N_2-passivated $In_{0.53}Ga_{0.47}As$ FinFETs," the team reports.

At 0.5V drain bias (V_{DS}), the sub-threshold swing (SS) was as low as 78mV/dec, and drain-induced barrier lowering (DIBL) was 55mV/V. Reducing the drain bias to 0.05V allowed even lower OFF-currents of 1.13×10^{-4}μA/μm. ■

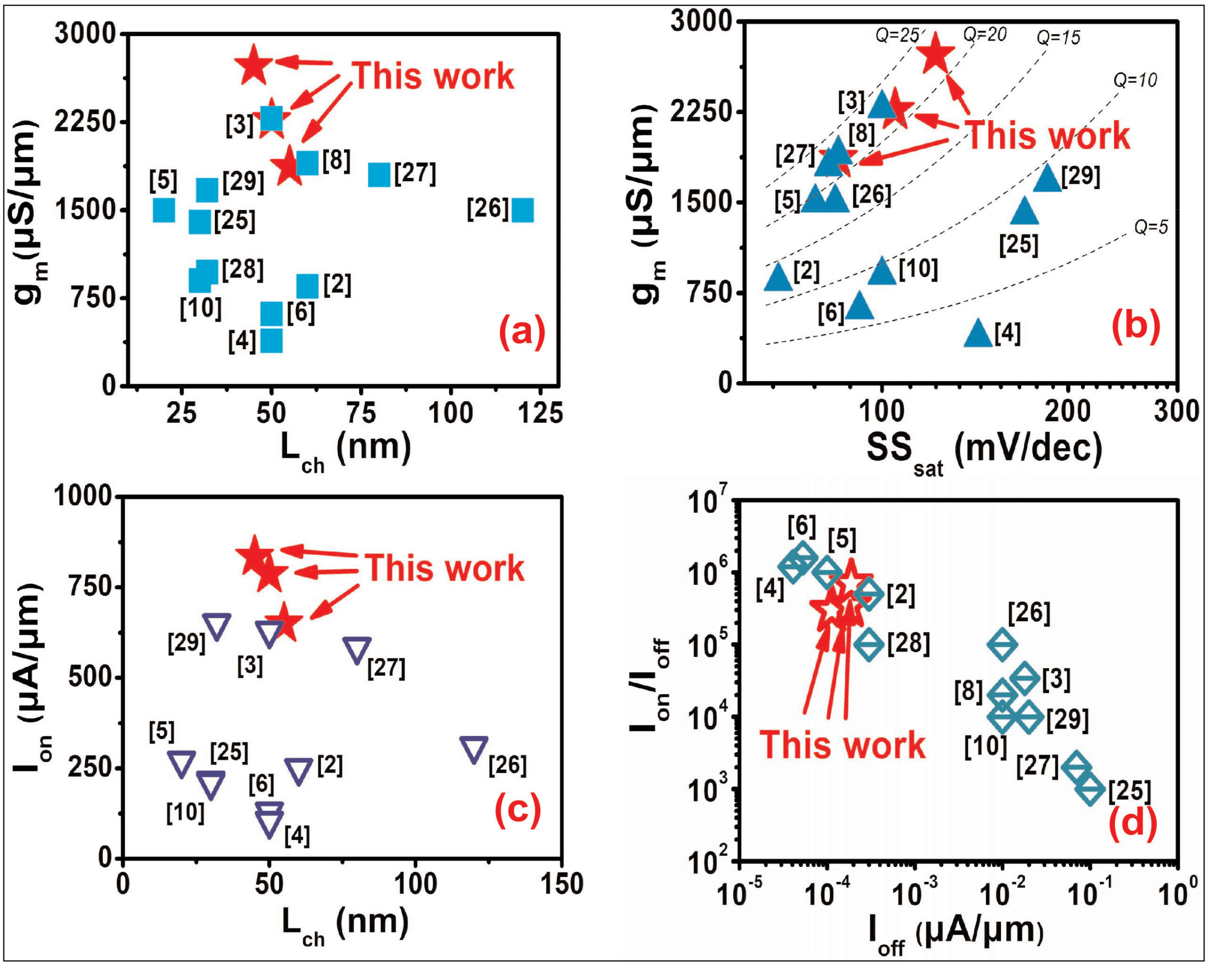

Figure 2. Benchmark plots of (a) peak gm versus channel length (L_{ch}), (b) peak g_m versus subthreshold swing (SS) in saturation regime, (c) I_{ON} at $V_{GS}-V_{th}$ = 0.5V and V_{DS} = 0.5V versus L_{ch}, and (d) I_{ON}/I_{OFF} ratio versus OFF-current. Data compared with other state-of-the-art $In_{0.53}Ga_{0.47}As$ FinFET devices.

https://doi.org/10.1109/TED.2021.3133222

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