Indium gallium arsenide one-transistor dynamic random access memory

Researchers hope for devices with lower operating voltages and lower energy consumption.

Spain's University of Granada and IBM Research Zürich in Switzerland have been developing III–V on silicon technology for dynamic random access memory (DRAM) based on one transistor (1T) and without a capacitor structure [Carlos Navarro et al, Nature Electronics, 2 (2019), p412]. The team comments: "Such capacitor-less DRAM has been demonstrated in silicon, but the use of other materials, including III–V compound semiconductors, remains relatively unexplored, despite the fact that they could lead to enhanced performance."

Removing the capacitor used in traditional '1T1C' DRAM allows simpler processing and should enable smaller cell sizes.

The increased carrier mobility in III–V compound semiconductors such as indium gallium arsenide (InGaAs) offers the prospect of lower operating voltages and lower energy consumption.

The researchers describe their structure as being related to the meta-stable dip RAM (MSDRAM) concept that uses parasitic floating-body effects (FBEs) to store information. FBEs arise in semiconductor-on-insulator

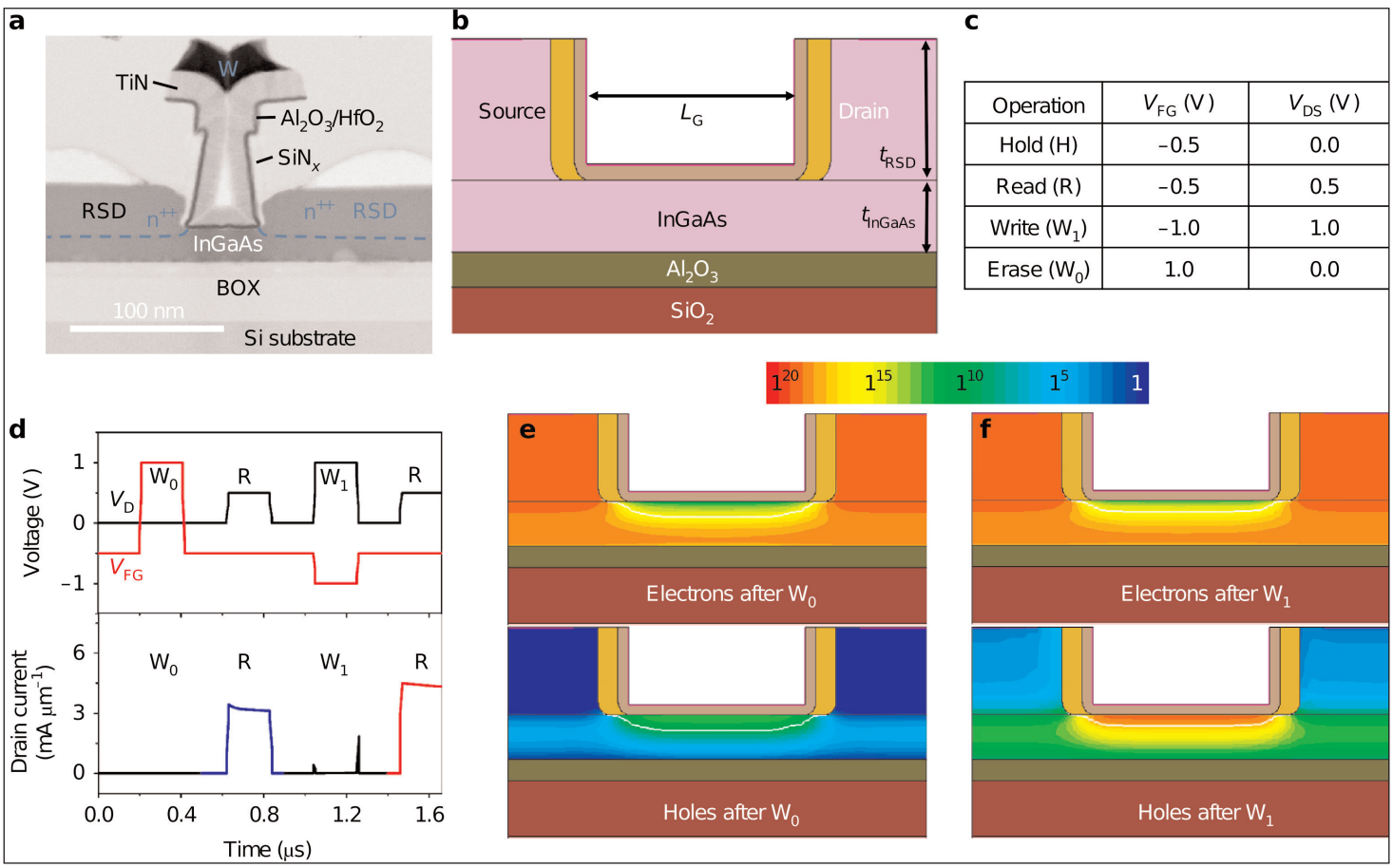

Figure 1. a, Transmission electron microscope image of III–V cell. b, Corresponding 2-dimensional structure used in simulations. c, Default front-gate (V_{FG}) and drain (V_D) voltages for memory operation. d, Readout drain current, demonstrating memory operation. Inset: drain and front-gate bias pattern. e,f, Electron and hole densities, after W_0 (e) and W_1 (f), respectively, demonstrating MSDRAM memory operation in structures similar to experimental devices with 5V on back gate. Simulated device dimensions: 90nm L_G, 1µm width.

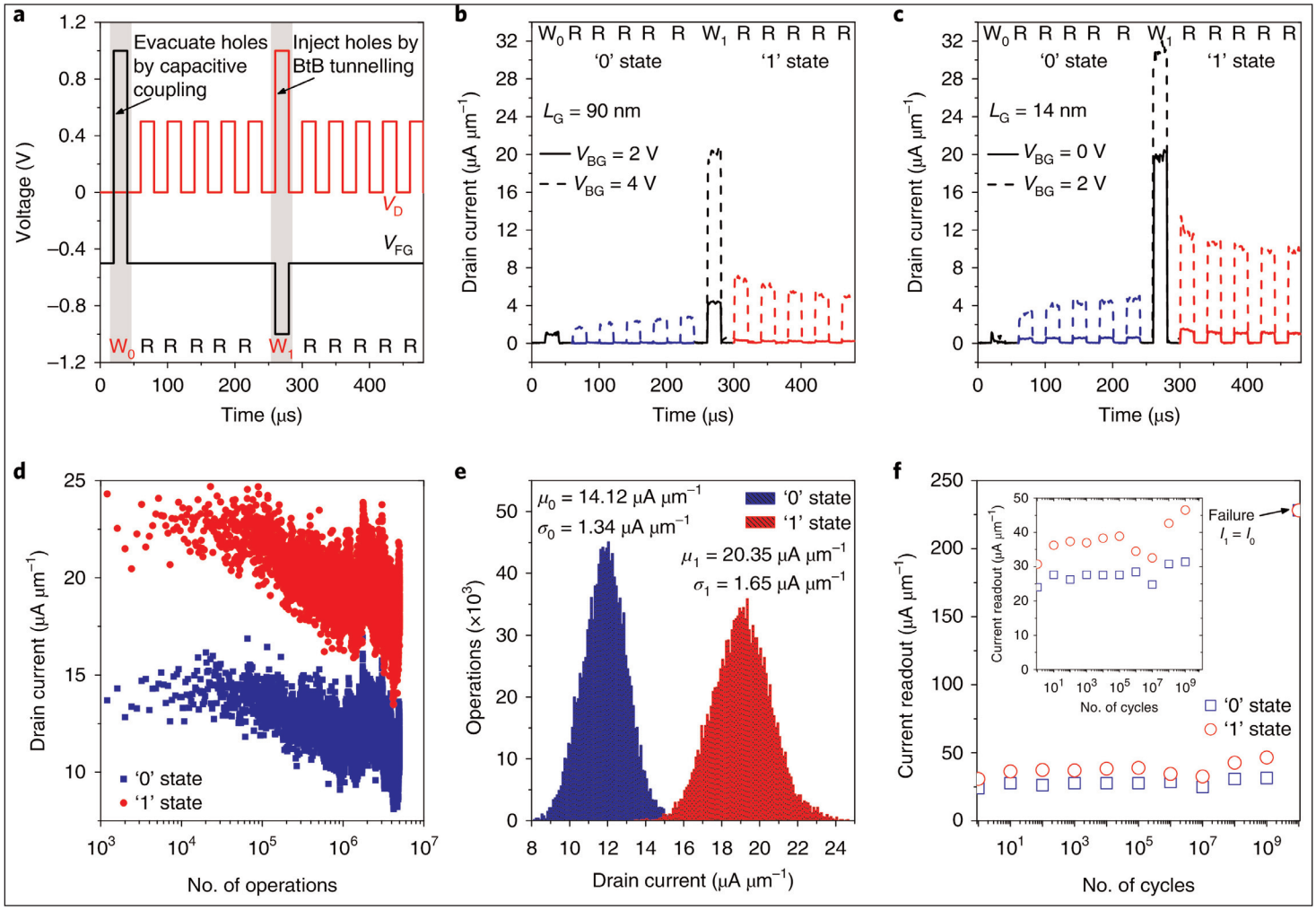

Figure 2. a, Default W_0–5xR–W_1_5xR sequence bias pattern to test memory operation. b,c, Readout drain current, successfully probing the memory behavior for 90nm (b) and 14nm L_G (c) at room temperature (300K). d,e, Endurance test on 50nm L_G device at high temperature (360K), showing continuous '0'- and '1'-state readout currents for the first 5x10^6 cycles (one in every 100 points) (d), together with Gaussian-shaped histograms (e). f, Longer cycling test showing memory operation up to between 10^9 and 10^{10} cycles when successive '1'-state writing steps are carried out at 50MHz. State current readouts characterized every decade. Inset: magnified view of memory operation

(-OI) structures where the potential in the semiconductor depends on biasing history and carrier recombination processes. The charge in the body of the device modulates current flow in the reading operation.

The team sees potential uses of the device coming from demands for higher performance and scalability, along with III–V optoelectronics and high-power circuitry.

The devices were based on InGaAs-OI transistors fabricated on silicon at IBM's Zurich facility (Figure 1). The InGaAs channel layer was 20nm thick. The indium mole fraction was 53%, which provides a good trade-off between the on- and off-current performance through a high electron mobility and a relatively wide bandgap.

InGaAs-OI on silicon wafers were direct bonded structures using metal-organic chemical vapor deposition (MOCVD) heterostructures grown on indium phosphide (InP) transferred to (001) silicon. The buried oxide layers (BOX) were added by atomic layer deposition (ALD) onto the InP growth wafer, which was then flipped onto the silicon for initial bonding, followed by annealing. The InP growth substrate, and etch stop layers, were then removed.

The aluminium/silicon BOX layers (10nm/25nm Al_2O_3/SiO_2) prevents charge leaked into the p-Si substrate. The back-side of the wafer served as a back gate electrode. A front gate was implemented with 4nm-total high-k aluminium/hafnium oxide (Al_2O_3/HfO_2) bilayer, giving a 1nm equivalent oxide thickness (relative to the traditional SiO_2).

The MSDRAM principle uses coupling between the front- and back-gates, along with floating-body and non-equilibrium effects. The gates create front- and back-channels. Holes accumulate in the front-channel, while the back-channel is driven into inversion by the back-gate. The accumulated holes modulate the electron density in the inverted back-channel. Larger hole density in the front-channel enables increased current flow in the inversion layer.

The '0' state is written (W_0 or 'erase') by applying a positive potential to the front-gate, expelling holes from the front-channel through capacitive coupling. The '1' state (W_1 or 'write') is created through band-to-band tunneling to inject holes from the drain edge with a negative front-gate potential and positive drain bias.

The MOCVD regrown n-type source/drain regions were raised 25nm and isolated from the gate stack with 9nm plasma-enhanced ALD silicon nitride spacers. The doping of the source/drain with tin was $2x10^{19}/cm^3$. The channel body suffered in performance due to some residual n-type doping of the order $2x10^{16}/cm^3$. This factor modified the desired MSDRAM behavior, to give something more approaching what is described as an 'A2RAM'.

Final devices with various gate lengths (L_G) were fabricated with a 0.5μm width. The subthreshold swings with the back-gate at 0V were ~150mV/decade and ~200mV/decade for 90nm and 14nm gate length, respectively. The relatively high swings were attributed to "interface defects at the gate/channel interface". The higher value for the 14nm device also indicated the presence of short-channel effects in the highly scaled device.

Putting a positive voltage on the back-gate switches the channel for current flow from the top to the back interface. This flattens the control of current flow by the top-gate. Due to the thick BOX layer, the current control by the back-gate is limited. However, the current in the back channel is modulated by charge trapped in the front channel, creating the prospect of 1T-DRAM performance (Figure 2).

The reading of the memory state was through a drain bias. Due to the residual body n-type doping, there was still a significant current flow for the '0' state, although the '1' state did demonstrate a higher value. Write and erase processes involved specific front-gate voltage pulses.

To test the endurance of the cell, a 50nm-gate device was subjected to $5x10^6$ cycles of a sequence of W_0–R–W_1–R operations at 360K without bit failure. The back gate was set at 5V. The various front-gate potentials were –0.3 V (R), –0.8V (W_1), and +0.8V (W_0). The pulse widths were 20μs. The researchers comment that basic calculations suggest that endurance of $5x10^9$ operations could be envisaged with nanosecond-order operations. Another test at 360K with 50MHz W_1 operations, considered the most damaging, only failed after 10^9–10^{10} cycles. ■

https://doi.org/10.1038/s41928-019-0282-6

Author: Mike Cooke