

III-nitride should enable access to high carrier density and high breakdown voltages.

The III-nitride semiconductor material consisted of a silicon substrate, 3.75 μm GaN buffer, 300nm GaN channel, 8nm aluminium nitride (AlN) spacer, and 23.5nm Al_{0.25}Ga_{0.75}N barrier. The two-dimensional electron gas formed at the top GaN interface with the spacer/barrier had $1.05 \times 10^{13}/\text{cm}^2$ carrier concentration, 1690 $\text{cm}^2/\text{V}\cdot\text{s}$ mobility, and 350 Ω/square sheet resistance.

The channel, source, drain and gate were fabricated using electron-beam lithography and inductively coupled plasma etch. Devices with varying parameters were defined. Annealed ohmic contacts to the source, drain and gate consisted of titanium/aluminium/titanium/nickel/gold.

This essentially two-step fabrication results in transistors with self-aligned gates. No insulation oxides or passivation layers were used. Such additions to improve performance are suggested as future work by Santoruvo and Matioli.

Wide-channel devices had larger maximum drain current and threshold voltage magnitude. The devices were normally-on, so the threshold was negative. The wider channels naturally had lower resistance. However, the narrower-channel devices had a further effect increasing resistance — strain relaxation in the AlGaIn barrier, decreasing carrier density due to reduced piezoelectric effects. Reducing the channel length also reduced resistance, giving similar increases in drain current and threshold.

The on/off current ratio was of the order 10^7 with less than 10pA leakage current for 210nm deep trench etching. Shallower trench etching to 140nm gave a slightly higher leakage, but still less than 100pA.

The shallower trenches also gave devices with more positive thresholds — i.e. the magnitude was smaller. This is attributed to an increase in gate capacitance for the shallower trenches.

Satoruvo and Matioli estimate the total effective capacitance of 0.7–3.9aF (where aF = atto-Farads = 10^{-18}F) for deep IPGFETs of widths 20–85nm. The corresponding values for shallow transistors were in the

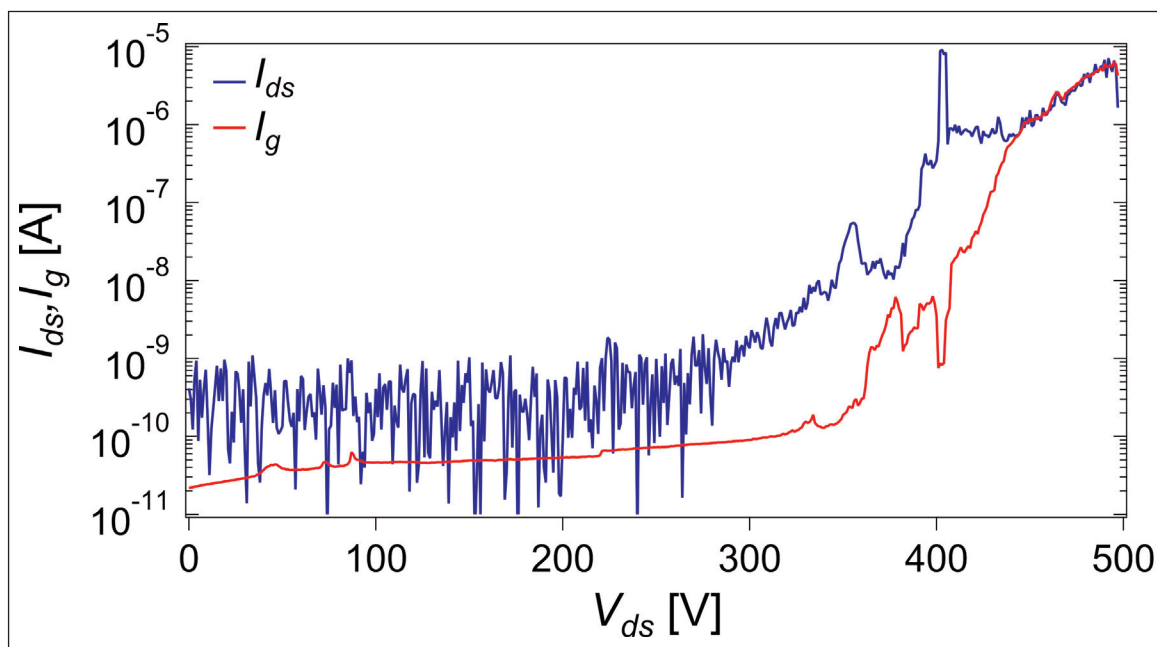


Figure 2. Drain and gate currents for 165nm-wide, 250nm-long IPGFET in -11V gate off-state.

range 2.2–9.4aF. “These are extremely small values of gate capacitance, which are very promising for high-frequency applications,” the researchers comment.

On the basis of these values, they estimate potential for up to 0.89THz cut-off frequencies, although the reported devices were not designed or tested for high-frequency performance.

A 50nm-long, 85nm-wide shallow IPGFET achieved a drain current of 1.4A/mm, which is 9x the value reported for similar structures using indium gallium arsenide (InGaAs) quantum well material. The improvement for GaN IPGFETs is credited to much larger carrier densities and very small sidewall depletion in III-nitrides.

Shallow 50nm-channel-length IPGFETs also demonstrated higher transconductance, which increased over a broader range of gate potentials with channel width. Normalized by channel width, the peak transconductance was 335mS/mm for 85nm-wide channels and 665mS/mm for 20nm. The latter value is 5x that of previous reports. The increase in normalized transconductance for narrower channels is attributed to improved modulation by the gate.

In the -11V gate potential ‘off’ state, leakage was maintained at a low level up to 300V (less than 1nA drain and 100pA gate current), breaking down at 500V (Figure 2). This performance trend was independent of channel width. “The similar behavior of I_{ds} and I_g suggests that at large voltages the leakage current flows entirely through the semiconductor buffer layers, not through the nanowires, since both the drain and gate contacts are ohmic,” Santoruvo and Matioli write. ■

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