Silicon-on-insulator substrates for compound semiconductor applications

Mike Cooke reports on research developments reaching towards high-power electronics and infrared optical communications.

Silicon-on-insulator (SOI) was developed in the silicon transistor industry to reduce parasitic capacitances in integrated circuits. As the technology developed, more applications and device structures benefiting from such substrates were demonstrated, such as micro-electro-mechanical systems (MEMS) and photonics.

In the past year, several research groups have reported on combining SOI with III-V compound semiconductors. One attractive feature is that SOI, and silicon, come in larger-diameter, lower-cost substrates than is standard for compound semiconductors. Further, combining SOI with III-V semiconductors could add new functionality to the conventional silicon complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) that power our digital age.

Gallium nitride (GaN)-channel transistors on SOI could add high-voltage or intense power density handling capability to silicon CMOS ICs in applications such as photovoltaic inverters, electric vehicle charging, and DC power transmission.

The insulation part of the SOI structure would provide vital electrical isolation to monolithic power circuits such as half-bridge layouts with transistors biased at significantly different levels. Such isolation is difficult when devices are placed on a common conductive substrate. At present, isolation is achieved by multi-chip modules that involve increased production complexity and cost.

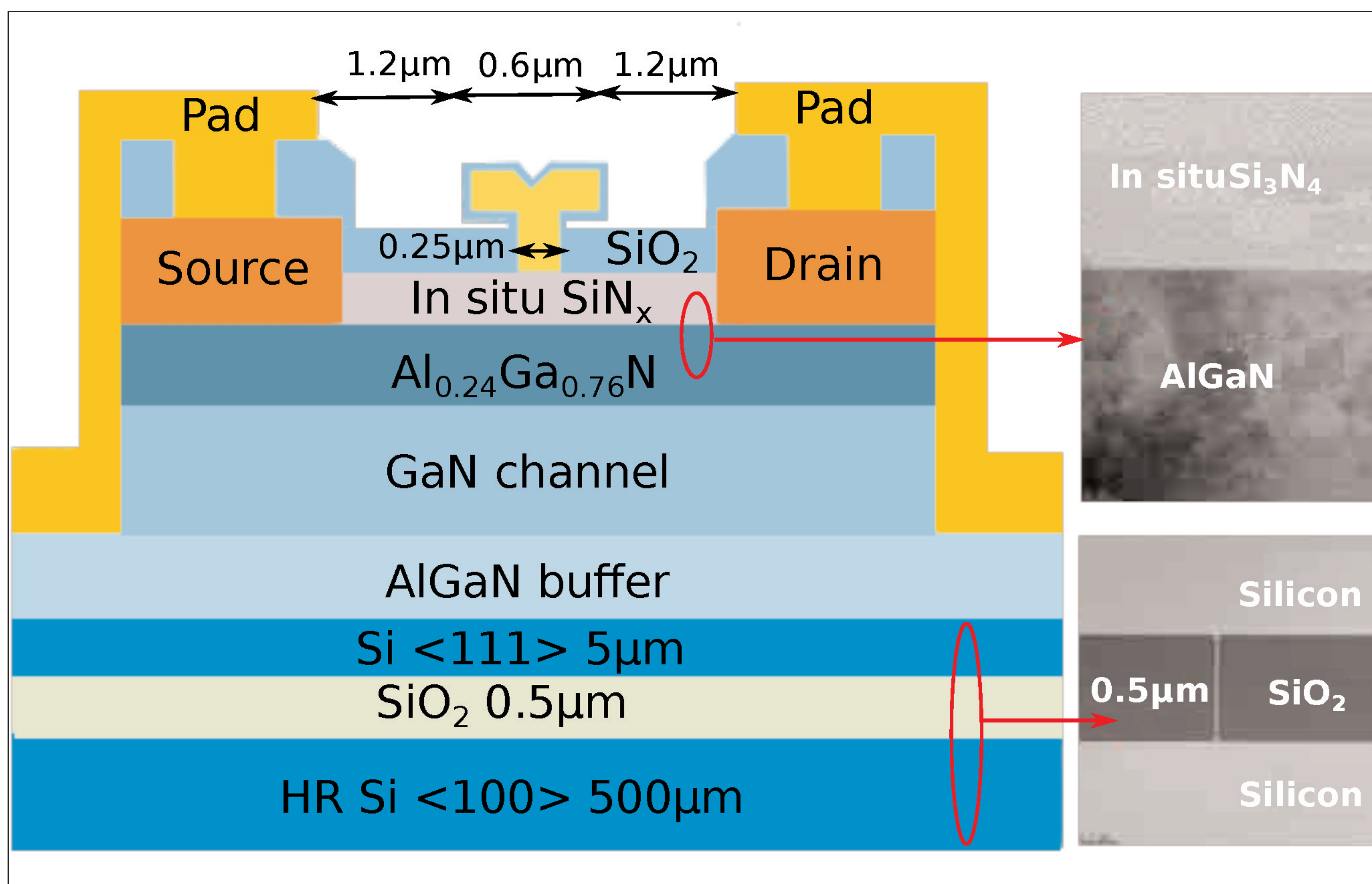

Figure 1. Cross-sectional structure of in-situ SiN_x/AlGaN/GaN MISHEMT on SOI substrate.

GaN is also used in radio frequency (RF) power devices, and again the insulator layer in SOI substrates provides opportunities for reducing power losses from currents induced in the substrate.

Both silicon and SOI have been used as the basis for photonics platforms, with the patterning of waveguides and other optical elements in advanced stages of development. The component lacking in this work is light- and laser-emitting devices. Here, integration of indium gallium arsenide phosphide (InGaAsP) alloys could lead to compact, low-cost optical communications components.

Aluminium gallium nitride transistors

Chang Gung University and Episil-Precision in Taiwan claim the first demonstration of in-situ silicon nitride (SiN_x) gate dielectric aluminium gallium nitride (AlGaN) barrier metal–insulator–semiconductor high-electron-mobility transistors (MISHEMTs) on 6-inch SOI substrates [Hsien-Chin Chiu et al, IEEE Transactions on Electron Devices, vol64, p4065, 2017].

The devices showed improved DC, dynamic and RF performance over the same structures grown on high-resistivity silicon (HR Si). The devices also included a SiN_x dielectric produced 'in-situ', immediately after the III-nitride deposition. Efficient RF performance needs resistive substrates to reduce induced power losses.

The team comments: "With some suitable thermal management solution or high-thermal sink package designs, the MISHEMT on SOI provides a high potential for millimeter-wave power amplifier applications."

Metal-organic chemical vapor deposition (MOCVD) created an epitaxial structure of a 1.75μm AlGaN buffer layer, 0.5μm GaN channel, 18nm $Al_{0.24}Ga_{0.76}N$ barrier, and in-situ 15nm SiN_x passivation. Optimization of the silane (SiH_4) and ammonia ratio ensured an atomically sharp interface between the barrier and passivation, according to the researchers. The passivation was designed to suppress surface nitrogen vacancies that degrade performance.

This structure was grown both on 500μm SOI and 1000μm HR Si substrates. The fabricated MISHEMTs (Figure 1) were mesa isolated with annealed titanium/aluminium/nickel/gold ohmic contacts and nickel/gold T-gates. The gate length was 0.25μm. The gate was centered in the 3μm source-drain gap. The devices were completed with plasma-enhanced chemical vapor deposition (PECVD) and etching of SiN_x passivation.

Hall-effect measurements showed the material on SOI to have better performance than that on HR Si (Table 1). The MISHEMT performances also suggested reduced numbers of interface traps: $1.13 \times 10^{12}/cm^2$-eV on SOI compared with $1.71 \times 10^{12}/cm^2$-eV on HR Si. The researchers attribute the improvements to higher structural quality and reduced buffer trapping.

Raman spectroscopy suggested that the GaN on SOI was strain-relaxed compared with the GaN on HR Si. X-ray analysis indicated smooth layer surfaces and abrupt interfaces between layers. Atomic force microscopy (AFM) showed a smoother SiN_x surface of 0.318nm root-mean-square roughness for the SOI sample, compared with 0.34nm for the HR Si structure.

Electrically, the use of SOI substrates improved the off-state leakage by more than one order of magnitude over the HR Si MISHEMTs. In both cases, the dominant leakage route was through the buffer. The subthreshold swing was 0.39V/decade (390mV/decade) for the MISHEMTs on SOI, compared with 0.44V/decade for HR Si. The maximum drain current and transconductance were found to be 15% and 13% higher, respectively, in the devices on SOI. The researchers attribute the improvements to the enhanced mobility on SOI. The devices were normally-on at 0V gate potential with pinch-off voltages at −6.6V and −6V for the SOI and HR Si substrates, respectively.

At increased temperature of 500K, the current flow in the MISHEMTs dropped due to scattering from lattice vibrations, according to the team.

Three-terminal breakdown measurements were made on devices with 6μm source–drain gap. The gate potential was at −12V in the pinch-off region. The MISHEMTs on HR Si had an off-state leakage five times that of the device on SOI below 200V drain bias. With a 1mA/mm leakage criterion, the breakdown (V_{BR}) was at 315V drain bias for the MISHEMT on SOI, compared with 270V for the HR Si structure.

The researchers comment: "The superior performance of the SOI can be attributed to the suppression of electrons being injected from the silicon substrate into the III-nitride/Si interface. Furthermore, the leakage current of traditional HR-Si substrates was dominated by space-charge-limited current conduction through the buffer/transition layers."

The V_{BR}^2/R_{on} figure of merit (R_{on}, on-resistance) was 11.84MW/mm for the SOI MISHEMT, while the SOI device registered 6.56MW/mm.

The SOI MISHEMT also demonstrated improved dynamic on-resistance performance under 50μs pulsed operation

Table 1. Hall-effect measurements.

Substrate	SOI	HR Si
Two-dimensional electron gas density	$1.02 \times 10^{13}/cm^2$	$9.2 \times 10^{12}/cm^2$
Mobility	$1605cm^2/V$-s	$1533cm^2/V$-s
Sheet resistance	392Ω/square	419Ω/square

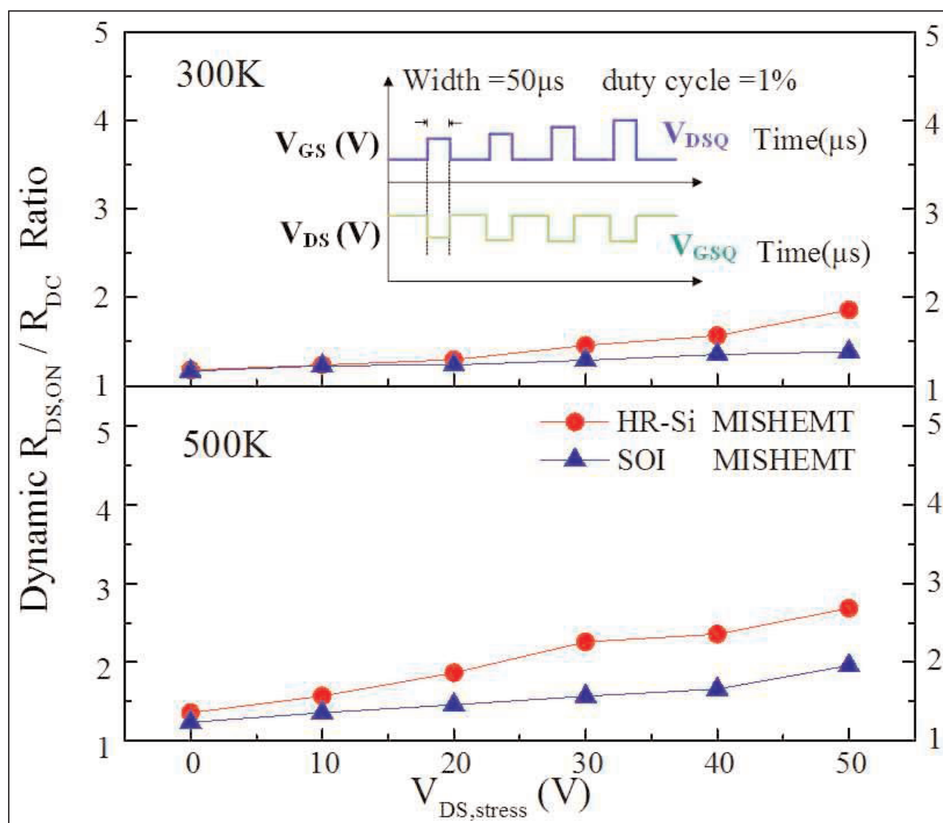

Figure 2. Dynamic switching performance determined with various stress voltages at 300K and 500K.

660mW/mm and 550mW/mm for SOI and HR Si substrate MISHEMTs, respectively. The power-added efficiency (PAE) reached around 30% for SOI and 20% for HR Si. "The increase of output power and the reduction of parasitic capacitances in MISHEMT on SOI provide a significant improvement in the device linearity," the team adds.

CMOS integration

Researchers in the USA have developed GaN high-electron-mobility transistors (HEMTs) fabricated on 200mm-diameter SOI substrates with multiple crystal orientations [Ko-Tao Lee, et al, IEEE Electron Device Letters, vol38, p1094, 2017]. The team from IBM's T. J. Watson Research Center, Massachusetts Institute of Technology, Veeco Instruments Inc and Columbia University hope that the work will lead to heterogeneous integration of GaN power transistors with high-speed CMOS devices.

The substrates consisted of 750μm Si in the (111) crystal orientation, 145nm of buried oxide (SiO_2) and 80nm Si (100). The Si (111) was used for the growth of GaN, while the Si (100) gives optimum performance for CMOS devices. Thermal oxidation of the Si (100) surface reduced the 80nm layer to 40nm. The researchers point out that this is the preferred thickness for state-of-the-art 14nm-node CMOS.

Reactive ion etch (RIE) was used to expose Si (111) window regions up to 200μm x 200μm for selective GaN growth (Figure 3). The total GaN coverage was

from the off-state (Figure 2). The increased dynamic on-resistance on HR Si was attributed to increased charge trapping in buffer states affecting performance.

Small-signal RF measurements gave cut-off/maximum oscillation (f_T/f_{max}) frequencies of 32.1GHz/51.9GHz and 18.3GHz/25.4GHz for the SOI and HR Si MISHEMTs, respectively.

Large-signal 2.4GHz RF measurements in AB-class amplifier operation gave maximum output powers of

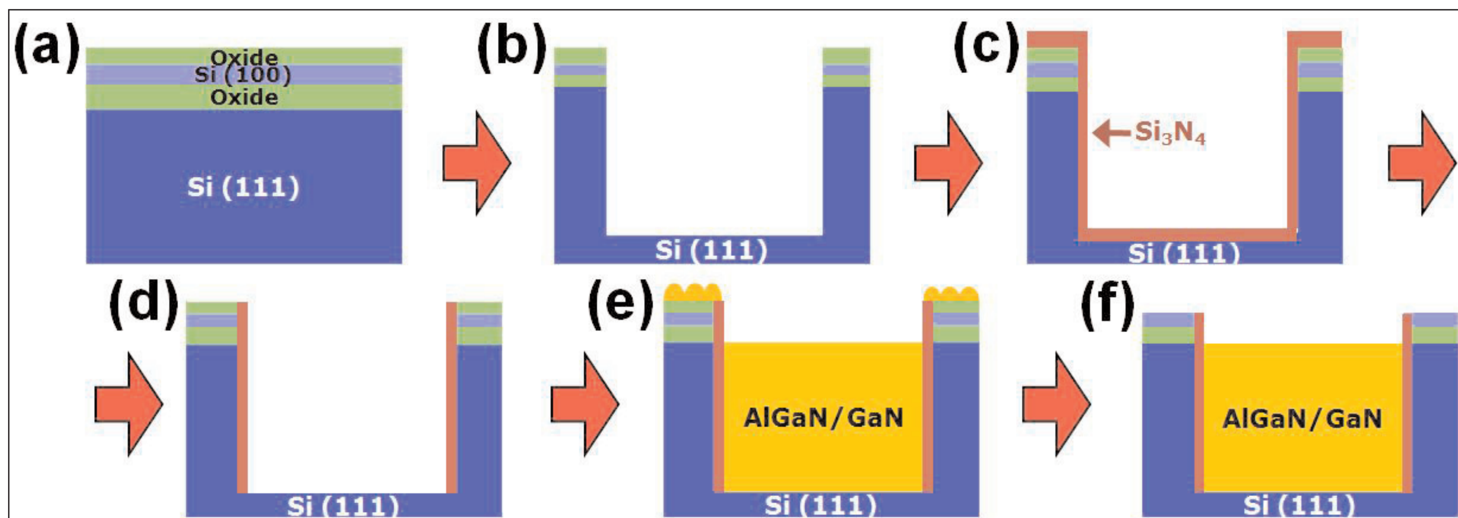

Figure 3. Hybrid-oriented SOI substrate with top Si (100) and bottom Si (111) preparation for MOCVD growth: (a) CVD-SiO_2 growth, (b) dry etching to expose Si (111) plane, (c) Si_3N_4 growth via CVD as isolation and diffusion barrier, (d) Si_3N_4 removal via dry etch to expose Si (111) plane, (e) AlGaN/GaN HEMT growth, (f) CVD-SiO_2 removal via chemical-mechanical planarization (CMP).

less than 50%, restricting bowing/warpage to within that needed for Si CMOS specifications (less than 50μm bow, for example).

The team comments: "The need for large-periphery high-power devices can potentially be achieved by combining multiple small patterned GaN devices. Once this approach is successful, this technology can extend the GaN-on-Si co-integration platform to high-power applications."

Silicon nitride (Si_3N_4) was deposited as a spacer on the window sidewalls, electrically isolating the GaN and Si (100) regions. The Si_3N_4 also provided a diffusion barrier, stopping Ga and Si atoms from doping the adjoining regions.

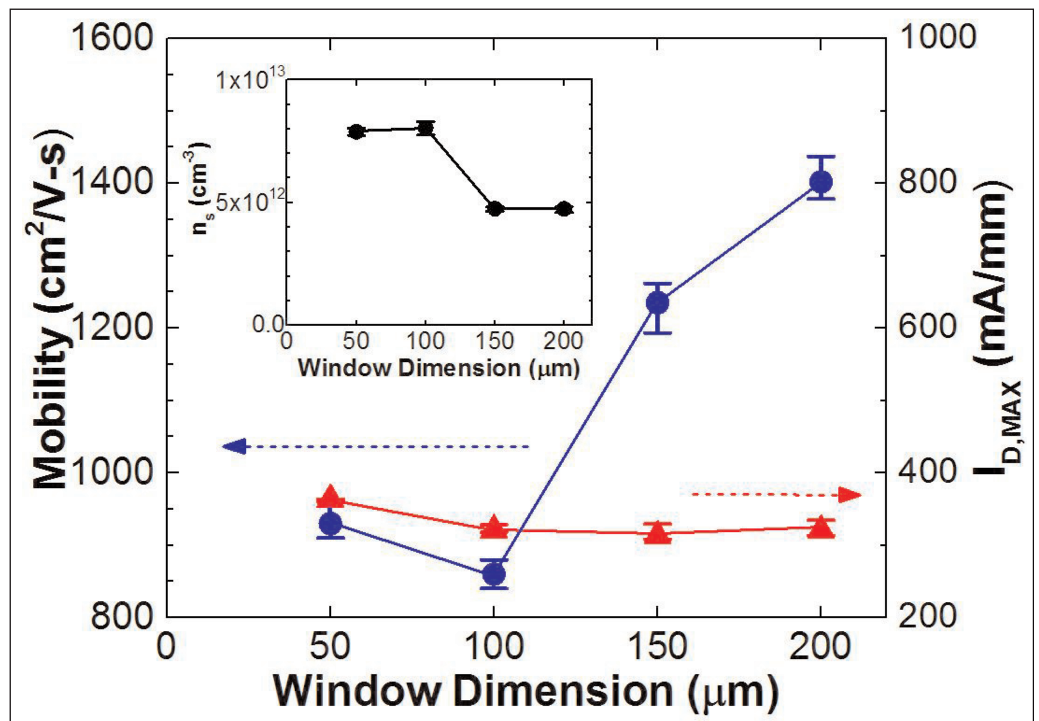

Figure 4. Electron mobility and drain current of GaN HEMTs from various window dimensions. Inset: corresponding carrier density (n_s) as function of window dimension.

The GaN and AlGaN material was grown by MOCVD: 130nm 1050ºC AlN nucleation, 1.5μm 1035ºC GaN buffer/channel, and post-growth ramp down to 985ºC to "facilitate unintentional [?] carbon doping". MOCVD for HEMTs added a 1nm AlN spacer, 20nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 3nm GaN cap.

A GaN layer grown on a Si (111) control wafer under the same conditions was only 0.6μm thick, less than half that of the 1.5μm layer in the SOI Si (111) regions. The increased thickness for the selective area growth was attributed to 'micro-loading effects' from the confined space of the Si (111) regions.

Standard HEMTs were produced with 3μm gate length and 3μm spacing between the gate and source and drain regions.

While the mobility varied according to the size of the window regions, declining with reduced size, the maximum drain current for the HEMTs was roughly constant (Figure 4). "The decline in electron mobility with decreasing window dimension is believed to be related to higher strain relaxation in smaller windows," the researchers explain.

Breakdown voltage was reduced with the smallest 50μm x 50μm windows (~40V versus ~80V for larger windows), which the researchers suggest could be due to defects at the GaN/Si_3N_4 sidewalls. By contrast, current collapse increased for the largest 200μm x 200μm windows (~25% versus less than ~6% for smaller windows). The quiescent state for the collapse measurements was −3V gate potential and 10V drain bias. The pulse width was 500ns. A 100μm x 100μm window device demonstrated a collapse of less than 2%. The researchers give 25% collapse as being typical for HEMTs on 'bulk' GaN.

The researchers comment: "The current collapse appears to correlate with the strain relaxation in patterned GaN, which is lower in smaller windows. Although the exact mechanism for this phenomenon needs further investigation, we believe that an interplay between defects and strain in patterned GaN dictates the observed current collapse behavior."

Isolation

Researchers based in Belgium and Finland have used SOI substrates to improve the electrical isolation of p-type GaN HEMTs [Xiangdong Li et al, IEEE Electron Device Letters, vol38, p918, 2017].

The researchers comment: "This work demonstrates that by using GaN-on-SOI in combination with trench isolation, it is very promising to monolithically integrate GaN power systems on the same wafer to reduce the parasitic inductance and die size."

It has also been found that growing GaN on SOI can result in higher-quality material, an effect that is attributed to the more compliant nature in terms of stress and strain of the insulator component of the wafer — silicon dioxide (SiO_2).

The 200mm-diameter SOI wafer consisted of a 1070μm (100) Si handle, 1μm buried SiO_2, and a 1.5μm (111) Si device layer. The SiO_2 thickness gave a balance between high breakdown voltage and low thermal resistance.

MOCVD resulted in 200nm aluminium nitride (AlN) nucleation, a 2.6μm (Al)GaN superlattice buffer, a

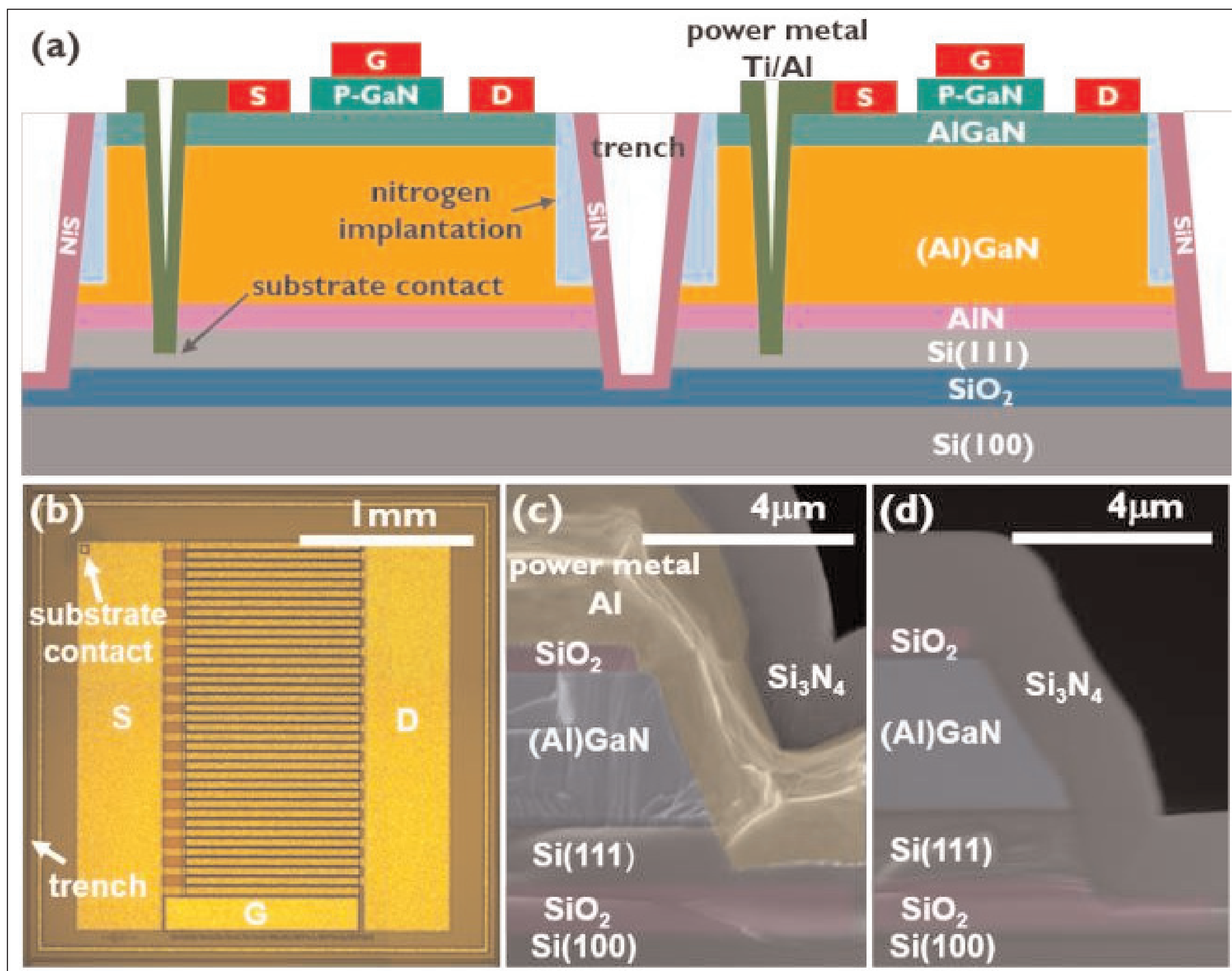

Figure 5. (a) Schematic cross section of enhancement-mode p-GaN HEMT, (b) top view of fabricated device, and cross-sectional secondary-electron micrographs of (c) substrate contact and (d) trench isolation fabricated on 200mm GaN-on-SOI.

300nm GaN channel, a 12.5nm $Al_{0.25}Ga_{0.75}N$ barrier, and 80nm of p-GaN. After deposition, the p-GaN layer was annealed in-situ in nitrogen to activate the magnesium doping, giving a hole concentration of $\sim 10^{18}/cm^3$.

The (Al)GaN buffer was designed to control stress and avoid wafer warpage (<50μm). Surface roughness was 1.4nm root-mean-square, according to atomic force microscopy.

The enhancement-mode (i.e. normally-off) p-GaN HEMTs (Figure 5) were fabricated with gold-free processing. Future integration with silicon electronic circuitry would need to eliminate gold from the production process, since the element poisons carrier transport in silicon.

The gate stack consisted of titanium nitride on p-GaN. Horizontal isolation was achieved with nitrogen ion implantation. A 50μm x 50μm substrate contact was created by etching through to the Si(111) device layer and sputtering titanium/aluminium, connecting the substrate with the ohmic source contact.

The device was completed with etching of a 20μm-wide isolation trench reaching down to the buried oxide and with deposition of a passivation layer. The trench isolation was found to have a horizontal breakdown voltage around 700V at 150ºC. The vertical breakdown of the buried oxide was around 500V at the same temperature.

The gate was 36mm wide and 0.8μm long. The distances between the gate and the source/drain were 0.75μm/6μm, respectively.

The gate threshold voltage was around +1.6V. A comparison device on non-SOI silicon had the same threshold. The comparison device did not have the substrate contact or trench isolation. The on-resistance of the comparison device was 10.6Ω-mm, and that of the SOI p-GaN HEMT was only slightly higher at 10.8Ω-mm at 0.1V drain bias and 7V gate potential.

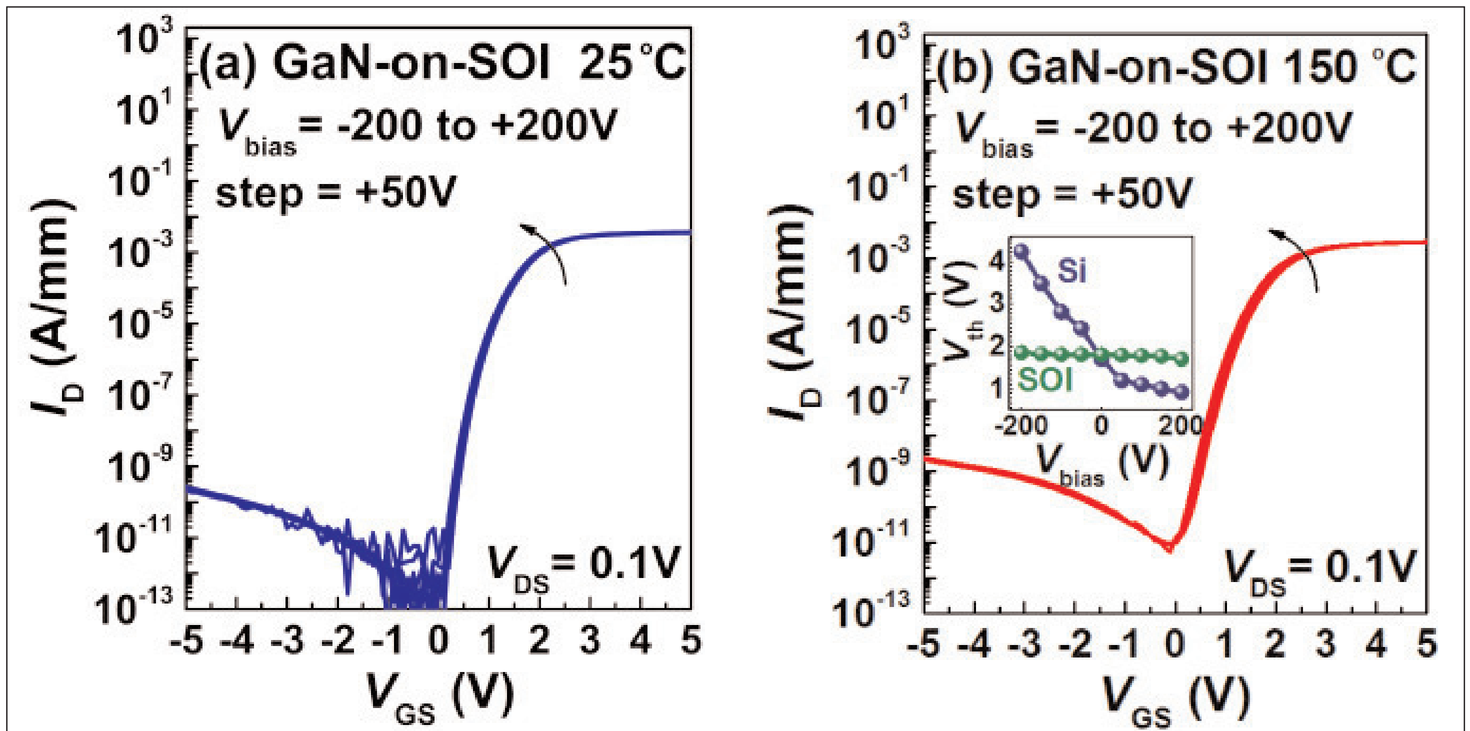

Figure 6. Evaluation of device isolation on GaN-on-SOI by measuring transfer characteristics while simultaneously biasing neighboring Si(111) device layer at different voltages at (a) 25ºC and (b) 150ºC.

The maximum drain current with 7V gate potential was 9A across the 36nm gate width, for both devices.

With the gate at 0V, the off-state breakdown for both devices was around 600V for 1μA/mm leakage. The researchers say that this gives sufficient margin for 200V-rated applications.

Where the SOI device improved on the comparison device was in the effectiveness of the electrical isolation. This was tested by biasing the substrate of the neighboring device between −200V and +200V (Figure 6). In particular, the SOI device's threshold voltage was stable over the bias range, while that of the HEMT on silicon varied by a few volts.

"With the demonstrated high-quality device isolation, it is very promising to achieve monolithic integration of GaN power system on GaN-on-SOI, and further explore the potentials of GaN in the field of high power applications," the team writes.

InGaAsP quantum wells

University of California Santa Barbara (UCSB) in the USA has developed the direct growth of InGaAsP multiple quantum well (MQW) nanowires on SOI substrates [Ludovico Megalini et al, Appl. Phys. Lett., vol111, p032105, 2017]. The target emission wavelength of the MQWs was 1550nm infrared, as favored for fiber-optic communication applications. The team looks forward to "integration of InP-based nanoridges in the SOI platform for new classes of ultra-compact, low-power, nano-electronic, and photonic devices for future tele- and data-communications applications."

SOI also has superior optical confinement properties compared to bulk silicon (Si): 13.4% confinement for SOI compared with 1.2% for silicon, according to InGaAsP nanowire simulations by the UCSB research team.

The SOI substrate used by UCSB had a 500nm lightly doped p-type Si layer on 1μm buried silicon dioxide. A 500nm PECVD silicon dioxide layer was used as a mask patterned with 3mm-long, 200nm-wide, 800nm-pitch stripes along the [110] direction. The wafer was then diced into 2cm x 2cm pieces.

The silicon device layer was etched with dilute potassium hydroxide at 70ºC to give v-grooves with {111} surfaces. A small undercut at the interface between the mask and device layer was found to be useful for trapping defects — in particular, stacking faults — in the subsequent InGaAsP growth by MOCVD.

The III-V layers consisted of 20nm of GaAs nucleation in two temperature steps of 410ºC and 430ºC, 430ºC InP nucleation, continued InP growth at 550ºC and 600ºC, and finally 650ºC growth of InGaAsP MQWs and 400nm InP cap (Figure 7). The InP nanowires were ~1.3μm thick with good height uniformity over a wide area, according to the researchers.

Photoluminescence experiments found a peak at 1555.7nm with 135nm full width at half maximum, attributed to the MQW structures. The pump power was 20.5W/cm^2. Lower pump powers gave a broader peak (Figure 8). This is attributed to saturation effects where the impact from defects becomes less significant at high excitation intensity.

The MQW layers were also non-uniform, leading to

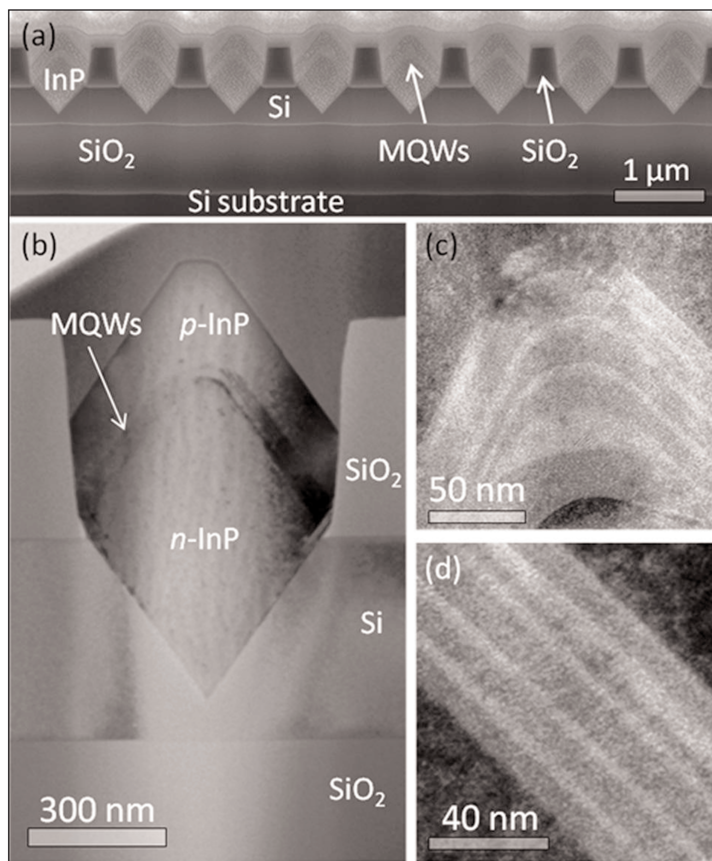

Figure 7. (a) Focused ion-beam scanning electron microscope (FIB-SEM) cross-sectional images of InP nanowires showing regular morphology. (b) Bright-field transmission electron microscope (BF-TEM) image of single nanowire with good symmetry. (c and d) BF-TEM images of QWs and barrier layers in (c) (001) surface and (d) {11-1B} facet. The dark colored layer is the barrier; the light colored layer is the quantum well.

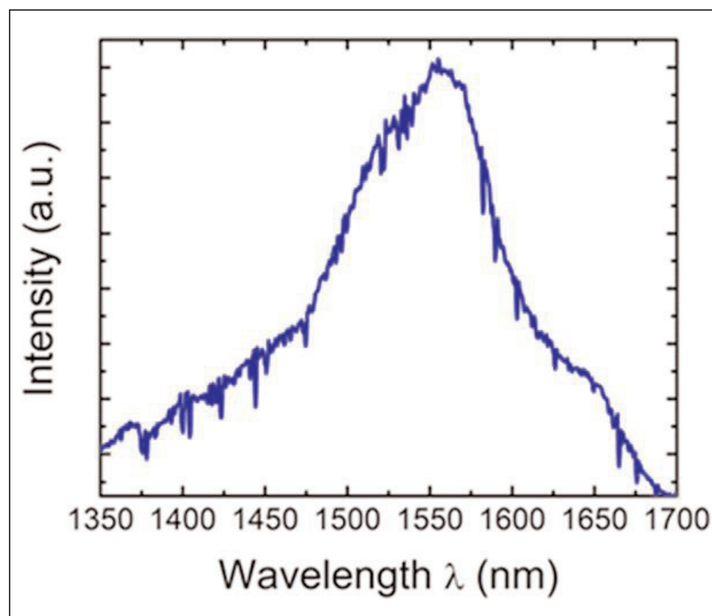

Figure 8. Photoluminescence spectrum showing emission at 1567nm from MQW structure inside indium phosphide nanowires grown on v-groove patterned SOI.

peak shifts and broadening as the excitation spot position varied over the sample. Inhomogeneous spectrum broadening could inhibit gain in laser devices. The researchers believe more uniform QWs could be achieved with careful adjustment of growth time and position within the nanowire. ■

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