Power & speed highlights for compound semiconductors

Mike Cooke reports on presentations given at the recent IEEE International Electron Devices Meeting.

High mobility and high breakdown voltages are key factors that different compound semiconductors offer future electronics, promising high speed and high power handling. However, wide-ranging commercial application is waiting for the right mix of technological advance and economic cost breakthrough.

The annual IEEE International Electron Devices Meeting (IEDM 2014) in San Francisco, CA, USA in December is a key event where such progress can be gauged. This year saw many reports of compound semiconductor research. Here we focus on power and high-speed electronics developments, along with optoelectronics. Finally, we look at some research into devices based on two-dimensional transition-metal dichalcogenide (TMDC) semiconductor layers – a topic that has recently become popular.

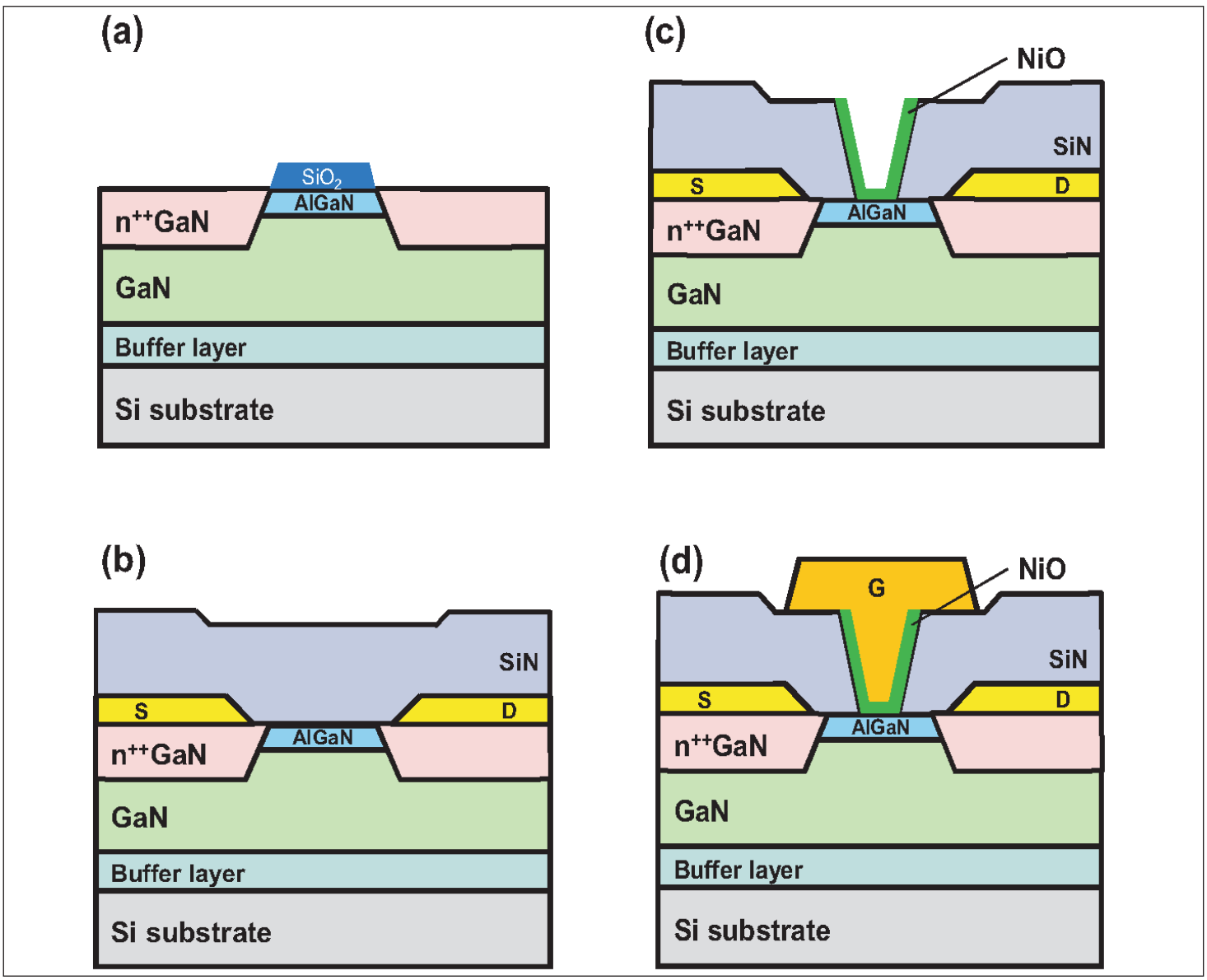

Figure 1. Processing steps of Panasonic/Kyoto normally-off GaN transistor: (a) selective re-growth of Ge-doped n^{++}GaN layer, (b) silicon nitride (SiN) deposition on device surface, (c) lift-off formation of NiO film using ALD, (d) gate metal deposition.

Power

Gallium nitride (GaN) is one compound semiconductor that is being developed for high power – both in terms of power switching and power amplification of radio-frequency/microwave signals. There is also much interest in growing the material on large-area silicon substrates to enable cost reduction.

For power-efficient fail-safe switching, normally-off transistors are desired — but difficult to arrange in GaN-based devices. Japan's Panasonic Corp and Kyoto Institute of Technology presented a normally-off GaN-based transistor with germanium (Ge) doped n^{++} GaN re-grown ohmic contact [session 11.1]. The researchers claimed a record-breaking on-resistance (R_{on}) of 0.95Ω-mm for their fabricated device. The maximum drain current and transconductance were 1.1A/mm and 490mS/mm, respectively. The threshold voltage was +0.5V and the on/off current ratio $5x10^6$.

The device (Figure 1) featured p-type nickel oxide (NiO) as part of the gate structure selectively grown using atomic layer deposition (ALD) in the 1μm source–drain gap. The nickel oxide gate footprint was 400nm. The presence of nickel oxide shifts the threshold to positive voltages, giving the desired 'normally-off' characteristic. The germanium doping allows electron carrier densities of $10^{20}/cm^3$, beyond those achieved with silicon doping.

Panasonic/Kyoto grew the heterostructure on silicon using metal-organic chemical vapour deposition (MOCVD). The ohmic contact re-growth was also through MOCVD. The barrier layer was 10nm aluminium gallium nitride ($Al_{0.3}Ga_{0.7}N$).

The researchers comment: "We believe the proposed GaN-based transistor will contribute to the drastic increase of conversion efficiency in DC-to-DC converters represented by POL (Point Of Loads)."

Another Panasonic group reported an extension of its GaN-based normally-off gate injection transistor (GIT) technology to 8-inch (200mm) silicon wafers and shorter gate lengths [session 11.3]. This Panasonic team also used indium aluminium gallium nitride (InAlGaN) quaternary alloy to reduce series resistance. Gate driver integration and flip-chip assembly were applied to deliver faster switching.

In terms of edging towards commercial acceptance, Transphorm Inc researchers in Japan and the USA claimed the first GaN HEMT on Si based cascode packages to pass Joint Electron Devices Engineering Council (JEDEC) qualification [session 2.6]. The researchers developed highly reliable 600V GaN HEMTs on silicon substrates. The devices in a cascode configuration package with high-voltage GaN HEMT and low-voltage Si MOSFET showed high breakdown voltages beyond 1700V with stable dynamic on-resistance. The researchers estimate a "conservative" mean time to failure (MTTF) of more than 10^7 hours at 600V.

Also, researchers from the wafer foundry giant Taiwan Semiconductor Manufacturing Co (TSMC) reported CMOS-compatible 100/650V enhancement-mode FETs and 650V depletion-mode MISFETs fabricated on 6-inch AlGaN/GaN-on-Si wafers [session 17.6]. The devices demonstrated high breakdown voltages of more than 820V and a low specific on-resistance of $4x10^{-6}Ω\text{-}cm^2$ with good wafer uniformity. The researchers stressed the need to optimize the epitaxial layers for improved device reliability.

Silicon carbide (SiC) is another popular material for potential future power electronics. Researchers at Toyota Central R&D Labs Inc, Japan's National Institute of Advanced Industrial Science and Technology (AIST) and the University of Yamanashi in Japan have been working to reduce feedback capacitance in SiC vertical junction field-effect transistors (VJFETs) [session 2.2]. Given the first listed organization, it is no surprise that potential applications include power conversion systems for hybrid electric vehicles (DC/DC converters, DC/AC inverters).

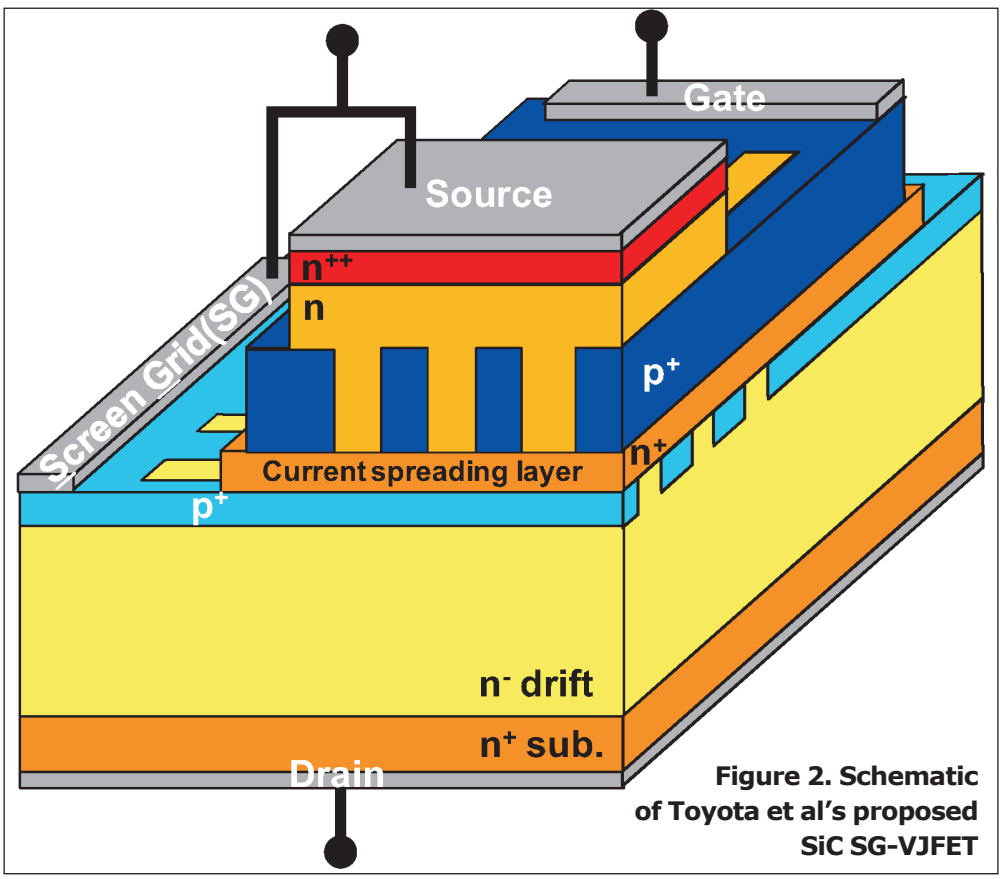

Figure 2. Schematic of Toyota et al's proposed SiC SG-VJFET

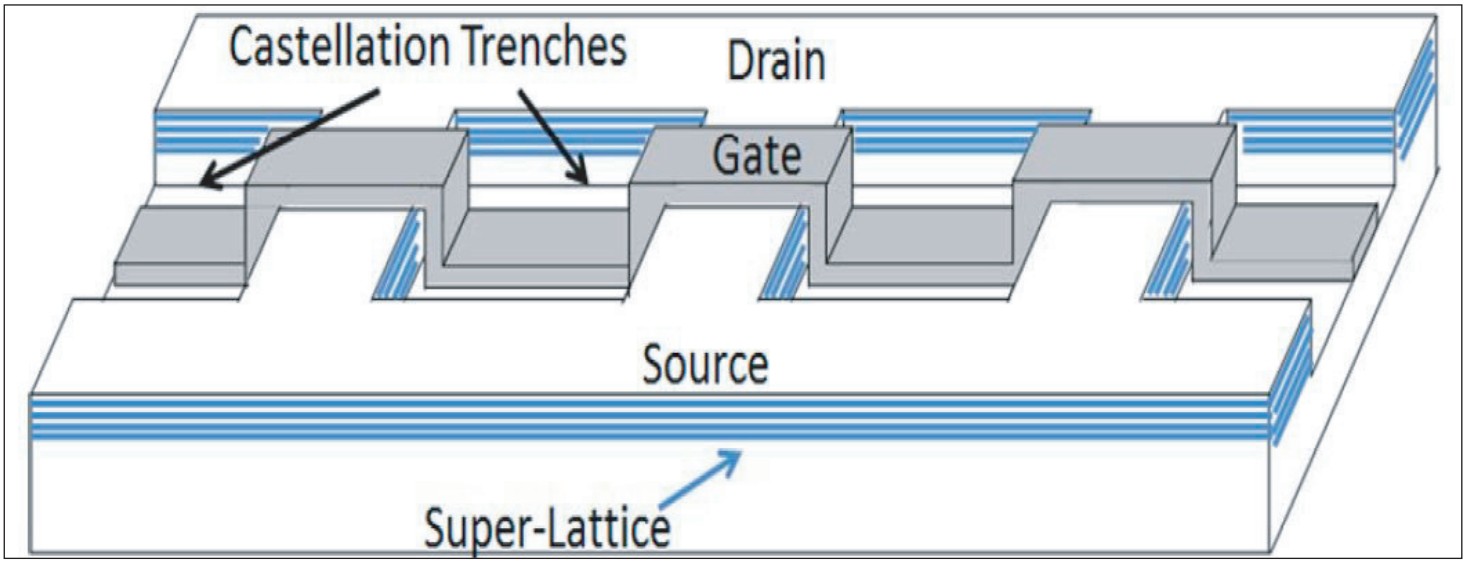

Figure 3. NGES' SLCFET device structure combining a super-lattice epitaxial channel with three-dimensional 'castellated' gate.

Feedback capacitance slows down the performance of VJFETs, compared with traditional MOSFETs. However, VJFETs tend to have better reliability and long-term stability. The new 'screen-grid' (SG-)VJFET (Figure 2) used a p^+ structure inserted between gate and drain to reduce feedback capacitance by about 80%, compared with a conventional VJFET (0.19nF/cm^2 versus 0.97nF/cm^2). The SG-VJFET also had lower feedback capacitance than a traditional MOSFET (0.38nF/cm^2).

In inductive-load double pulse tests the low feedback capacitance and high switching speed capability of the SG-VJFET enabled the lowest total power dissipation compared with traditional SiC devices.

RF GaN

Northrop Grumman Electronic Systems (NGES) presented a 'super-lattice castellated field-effect transistor' (SLCFET) [session 11.5]. The device features a GaN super-lattice channel with a 3D gate. The median maximum drain current was more than 2.7A/mm. The pinch-off voltage was –8V. The on-resistance (R_{on}) was 0.41Ω-mm and the off-capacitance (C_{off}) was 0.19pF/mm.

The researchers see the device being used in phase shifters, attenuators, true time delay, filters and transmit/receive (T/R) RF switches. Such systems are applied to advanced phased-array radars, multi-function sensors, and wireless consumer electronics.

FETs are desirable to achieve low power consumption, fast switching, modest control voltages and reliability (features that are lacking in RF MEMS or diode systems).

Switch applications need low insertion loss (when on) and high isolation (when off). FETs tend to offer poorer performance when compared with RF MEMS and diode devices. Attempts to improve insertion loss (R_{on}) tend to adversely impact isolation (C_{off}), leading to a figure of merit F_{CO} ($1/2\pi R_{on}C_{off}$).

NGES' SLCFET had an F_{CO} of 2.1THz, compared with 2.4THz for diodes and 3.8THz for RF MEMS. Slow phase-change switches can have F_{CO} up to 12.5THz. Transistor-based devices tend to have F_{CO} of the order of hundreds of gigahertz — e.g. 840GHz for indium phosphide (InP) HEMTs.

The superlattice channel stacks a series of two-dimensional electron gas (2DEG) conducting layers to reduce on-resistance. A three-dimensional (3D) gate with a series of 'castellation trenches' ensures that the channel can be turned off (Figure 2). The gate wraps around the channel, allowing the electric field to penetrate into the channel layers. The structure reduces R_{on} while maintaining the C_{off} value.

"The combination of this super-lattice epitaxial structure in conjunction with the castellated, three-dimensional gate is, to the best knowledge of the authors, a new device topology for FETs," the NGES team writes.

NGES demonstrated the device using an AlGaN/GaN heterostructure grown by metal-organic chemical vapor deposition on semi-insulating SiC. A single heterostructure had a sheet resistance of 300Ω/square — this was reduced to 60Ω/square for a superlattice structure.

Although the structure was not designed or optimized for high-frequency performance, the f_T cut-off frequency was 52GHz and the f_{max} maximum oscillation was 53GHz.

Wideband single-pole double-throw (SPDT) RF switch monolithic microwave integrated circuits (MMICs) for 1–18GHz operation in a series-shunt circuit topology achieved insertion loss less than 0.1dB and isolation greater than 26dB. The researchers say that this compares favorably with the performance of RF MEMS and diodes.

"By combining excellent RF switching performance with the numerous desirable aspects of FET based switching, the SLCFET is a key enabling technology for next-generation RF systems," the researchers conclude.

High speed

Indium gallium arsenide (InGaAs) is the most common compound semiconductor option being explored for high-mobility electronics. Massachusetts Institute of Technology (MIT) claimed a record transconductance ($g_{m,max}$) of 3.1mS/μm and R_{on} of 190Ω-μm in 80nm-gate-length self-aligned tight-pitch InGaAs quantum-well MOSFETs (QW-MOSFET) [session 25.1]. The result came as part of study led by Jesús A. del Alamo into the effect of scaling channel thickness (t_c) and metal contact length (L_c) using a fabrication process that features precise dimensional control. The channel thickness for the record transconductance was 9nm. The drain bias was 0.5V. The researchers believe their work could lead to III-V MOSFET high-performance applications.

In particular, the MIT team also claimed the first working front-end device structures with 40nm contacts and 150nm gate-to-gate pitch. The researchers say sub-150nm pitch "is a significant leap in an effort to meet the requirements of the ITRS 2013 roadmap for III-V CMOS logic." Up to now, the densest III-V devices have tended to have around 500nm pitch.

Thick t_c (11nm) allowed increased mobility to 8800cm^2/Vs. "To the authors' knowledge, this is the highest μ_{eff} in an InGaAs/InAs-channel MOSFET," the team writes. By contrast, a thin t_c gave better control of short-channel effects (SCEs). A 4nm t_c enabled a reduction in subthreshold swing to 111mV/decade, compared with 159mV/decade for a 9nm t_c.

The devices (Figure 4) used a contact-first technology developed at MIT. The channel thickness t_b was controlled by reactive-ion and digital etching. The digital etch process allows nanometer-scale precision. The initial 10nm composite channel consisted of (top to bottom) 3nm $In_{0.7}Ga_{0.3}As$, 2nm InAs, and 5nm $In_{0.7}Ga_{0.3}As$. Above the channel was a 3nm InP barrier.

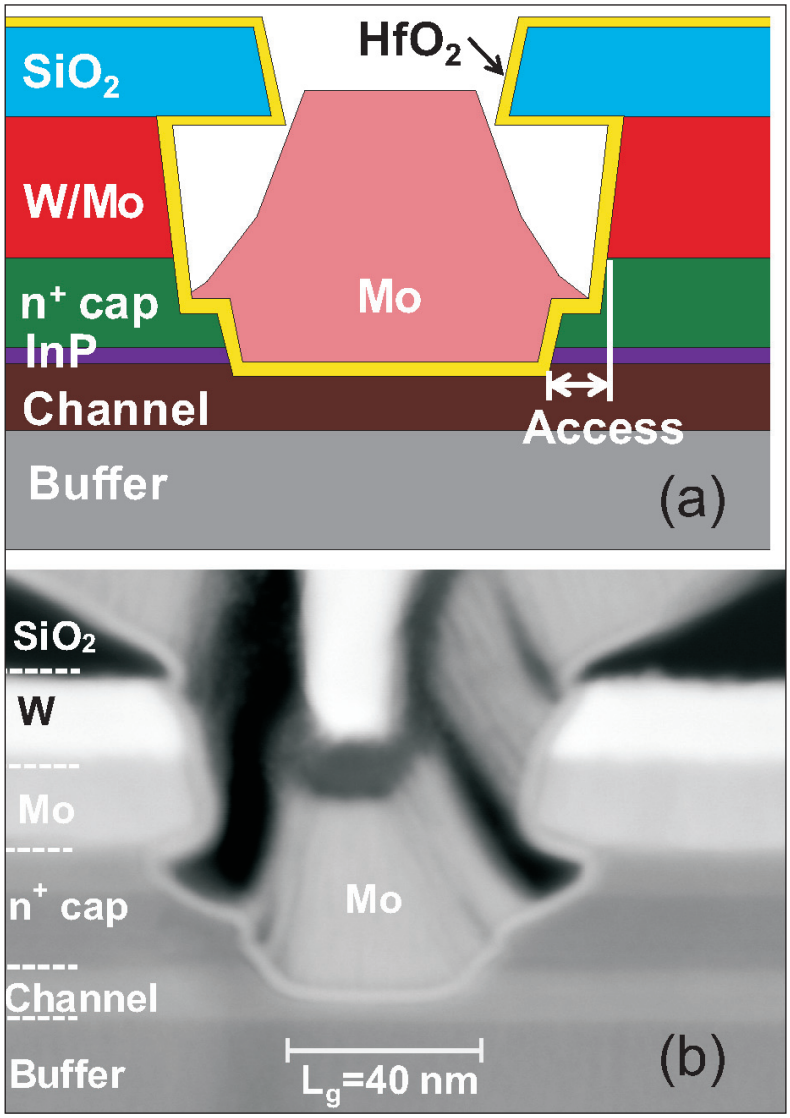

Figure 4. (a) MIT InGaAs MOSFET cross-section schematic, and (b) TEM of complete device with 40nm gate length and 2.5nm hafnium dioxide (HfO_2) gate dielectric.

The contacts consisted of molybdenum on n^+-InGaAs cap with a resistivity of $(8\pm2)\times10^{-9}\Omega.cm^2$. Studies of the effect of scaling the contact length gave a contact resistance of 70Ω-μm for 40nm-long contacts. "These are encouraging results but more research is required to attain the required R_c in nanometer-scale contacts," the researchers comment.

Another group led by Jesús A. del Alamo at MIT claimed the first InGaAs/InAs heterojunction single nanowire (NW) vertical tunnel FETs fabricated by a top-down approach [session 25.5]. The fabrication involved III-V dry etching and a new technique for gate–source isolation.

The resulting devices were 50nm-diameter NW TFETs with a channel length of 60nm and equivalent oxide thickness of 1.2nm. The average subthreshold swing of the devices was 72mV/decade at 0.5V drain bias over two orders of magnitude of current. At 0.3V operating voltage, the on-current was 0.27μA/μm with a fixed off-current of 10^{-4}μA/μm. The researchers comment: "This is the highest on-current demonstrated at this off-current level in NW TFETs with III-V materials."

Short-channel effects are often tackled using three-dimensional structures such as gates that wrap around a fin (fin-FET). Unusually, Singapore's Nanyang Technological University and Institute of Materials Research and Engineering (IMRE), along with Ohio State University in the USA, used stress engineering to achieve simultaneous high performance in triple-gate fin-HEMTs (Figure 5) produced using InAlN/GaN on silicon substrate rather than in InGaAs fin-FETs [session 25.6]. The stress was introduced using a silicon nitride passivation layer.

The on-current, off-current, extrinsic transconductance, SS and drain-induced barrier lowering (DIBL) demonstrated record values of 1.03A/mm, 1.13μA/mm, 645mS/mm, 82mV/decade and 28mV/V, respectively,

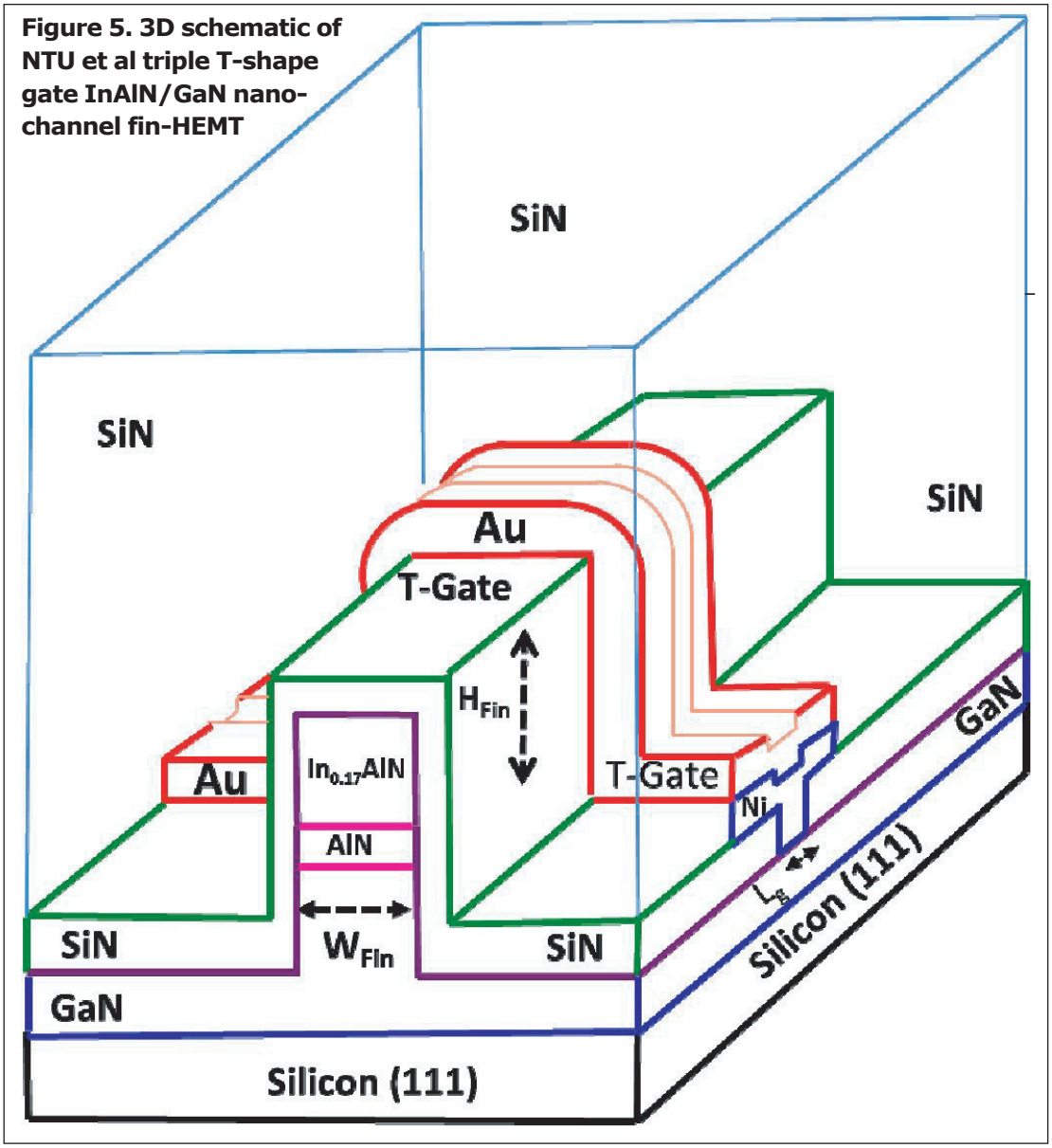

Figure 5. 3D schematic of NTU et al triple T-shape gate InAlN/GaN nano-channel fin-HEMT

at 0.5V drain. The researchers pointed out that their high-performance device used more relaxed device geometries such as 170nm T-gate compared with ~80nm I-gates on 88nm fins. The effective nano-channel width was 200nm. The researchers see their devices as promising for future ultra-high-speed device applications.

The team also claims its work as the first report of a T-gate approach on GaN-based fin-HEMTs. The maximum Q-factor consisting of the transconductance to subthreshold swing ratio was 7.9 at 0.5V drain, compared with less than 2 for a conventional GaN HEMT.

Opto

Another unusual report was of light emission from metal/semiconductor 'Schottky' junctions rather than the usual heterostructures of semiconductor materials. Hong Kong University of Science and Technology (HKUST) reported on its work generating GaN band-edge ultraviolet electroluminescence at 364nm from a forward-biased metal-AlGaN/GaN Schottky junction at room temperature [session 11.4].

A Schottky-on-heterojunction light-emitting diode (SoH-LED) in combination with a GaN HEMT driver achieved switching at up to 120MHz, "adequate for providing optical control signals for GaN high-side power switches," according to HKUST.

The team sees the technology as having potential for high-speed on-chip light-sources integrated with GaN electronics. The researchers have also demonstrated an AlGaN/GaN high-electron-mobility light-emitting transistor (HEM-LET).

The AlGaN/GaN heterostructure is being widely developed for power high-frequency and switching electronics (see above). Optocouplers are applied in high-voltage switching circuits, providing isolation between low-voltage control circuitry and high-voltage drive currents. The HKUST team comments: "An opto-coupler that is material/process compatible and can be seamlessly integrated with the AlGaN/GaN-based power electronic devices/circuits is highly desirable for an all-GaN solution that promises reduced parasitics, compact size and enhanced reliability."

Although photodetectors for AlGaN/GaN circuit integration have been developed, until recently compatible light sources have not been available. "For the first time, we demonstrated that the metal-AlGaN/GaN Schottky diode is capable of producing GaN band-edge UV emission at 3.4eV/364nm under forward bias larger than ~2V at room temperature," the HKUST team maintains.

The devices (Figure 6) were grown on (111) silicon using metal-organic chemical vapour deposition. The AlGaN barrier surface was plasma treated before anode deposition to remove native oxide and for nitridization. The devices were also annealed after fabrication.

Spectral analysis of the electroluminescence (EL) showed that the source of the emission was the GaN

part of the heterostructure, with no light coming from the AlGaN barrier layer. The current and light thresholds for the diode were at 1.1V and 2V, respectively.

The light threshold is about 1.4V lower than would be naively expected from the GaN bandgap of 3.4eV, indicating "an abnormal anti-Stokes light emission process". Anti-Stokes processes are usually associated with photons that pick up energy from lattice vibrations/phonons in addition to the energy change of the generating electron.

The researchers suggested two possible models for the anti-Stokes effect: "one electron ionizes the upper (Fermi-level de-pinning) or lower (Auger process) surface-band state, inducing the generation/injection of one hole to recombine with another electron. This 2e–1h process maintains energy conservation and explains the anti-Stokes characteristic of EL emission."

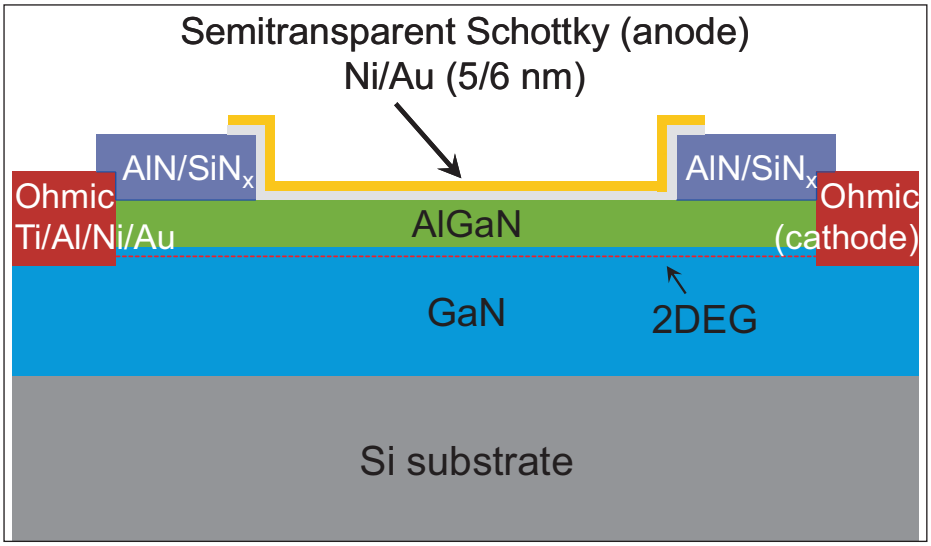

Figure 6. Cross-section of HKUST SoH-LED on AlGaN/GaN-on-Si.

2D semiconductors

Although graphene has for a while dominated 2D electronics research, interest is growing in transition-metal dichalcogenide (TMDCs) such as molybdenum or tungsten compounded with sulfur or selenium to give MoS_2, $MoSe_2$, WS_2 or WSe_2.

One challenge has been to make low-resistance contacts with external probes. Gwangju Institute of Science and Technology in South Korea achieved a low contact resistance for MoS_2 FETs using an interlayer of titanium dioxide (TiO_2) to achieve Fermi level de-pinning [session 5.1]. The value of contact resistance was ~5.4kΩ-μm, about five times lower than for devices without an interlayer. Maximum drain current was increased up to 2.51μA/μm with 0.5V drain bias — 10–20 times higher current drivability compared with prior results, say the researchers. The gate voltage was 20V above threshold.

The devices were produced by mechanical exfoliation using Scotch tape onto silicon/silicon dioxide substrates

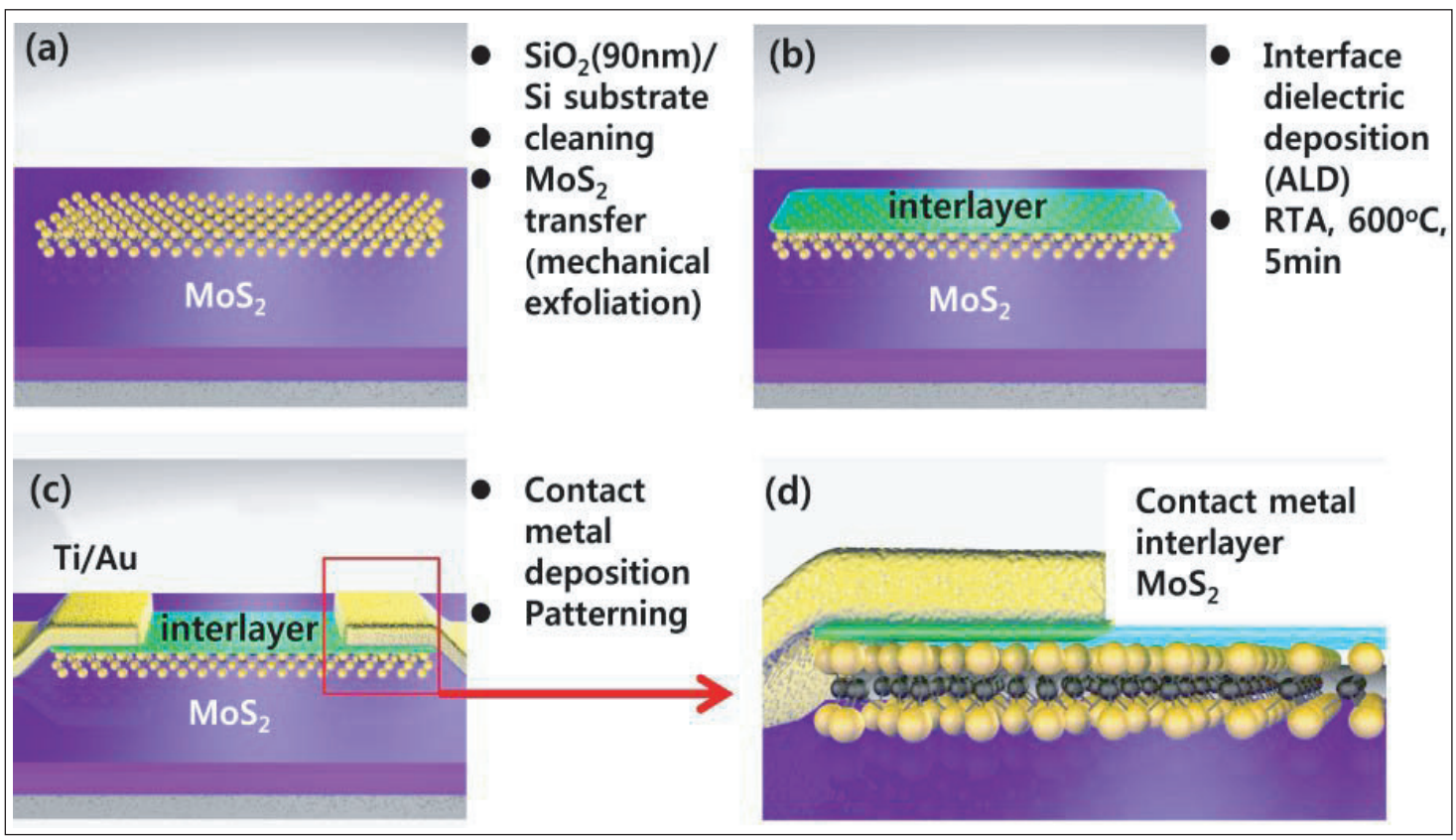

Figure 7. Gwangju fabrication flow and schematic of MoS_2 back-gate FET with insulating interlayer.

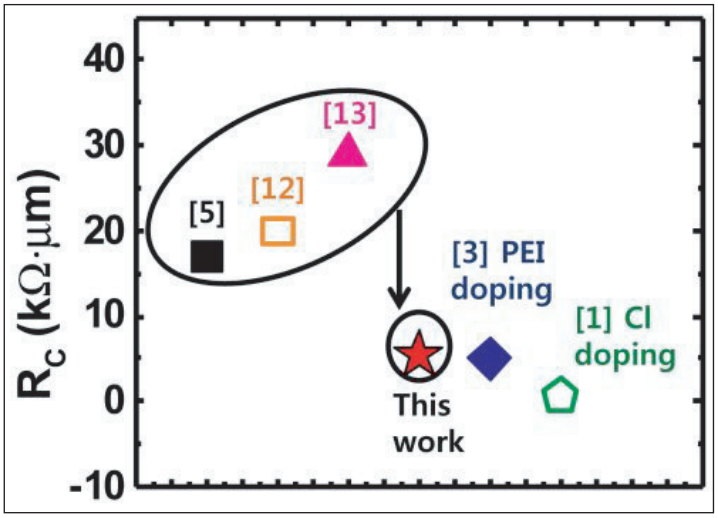

Figure 8. Benchmarking of Gwangju contact resistance against the achievements of other groups.

(Figure 7). The Scotch tape residues were removed with isopropyl alcohol (IPA) and rapid thermal annealing.

The best results were for a 2nm TiO_2 interlayer, although the researchers also tried aluminium oxide (Al_2O_3). The 2nm TiO_2 interlayer transistors had a 90nm equivalent oxide thickness for the gate insulation and a channel length of 3μm.

The Schottky barrier height was measured at 0.09eV for a 2nm TiO_2 interlayer, compared with 0.18eV for no interlayer and 0.13eV for a 2nm Al_2O3 interlayer. The improvement of TiO_2 over Al_2O_3 was attributed to differences in the interface dipole layer.

Some groups have reported lower contact resistances (Figure 8), but the Gwangju group point out that they did not use any doping of the MoS_2 to improve the contact. "We expect further improvement with addition of a proper doping process on the MoS_2 side," the researchers say.

Taiwan's National Chiao Tung University, Academia Sinica, and National Chiao Tung University claimed the first p-channel metal dichalcogenide ultrathin-body phototransistor (UTB-PT) with a response time as fast as 100μs [session 5.7]. The dichalcogenide channel material was large-area WSe_2 produced using CVD on sapphire. The researchers believe the device has "excellent compatibility with mass production", and propose its use in high-speed proximity interactive displays.

Collaboration between researchers based in Taiwan, Saudi Arabia and USA has resulted in CMOS-compatible stackable hybrid Si/MoS_2 3DFETs [session 33.5]. The various institutions involved were National Nano Device Laboratories in Taiwan, King Abdullah University of Science and Technology in the Kingdom of Saudi Arabia, Tamkang University in Taiwan, National Chiao-Tung University in Taiwan, Academia Sinica in Taiwan, and University of California Berkeley in the USA.

These researchers used Si/MoS_2 structures to produce double-channel fin- and nanowire-FETs (Figure 9). The MoS_2 consisted of between 3 and 16 molecular layers. The addition of MoS_2 increased the on-current by 25% over a pure silicon nanowire-FET.

The researchers believe that heterogeneous hybrid Si/2D electronic double-channel 3DFETs could enhance scaled device performance in applications that require technology more advanced than 7nm CMOS technology. ■

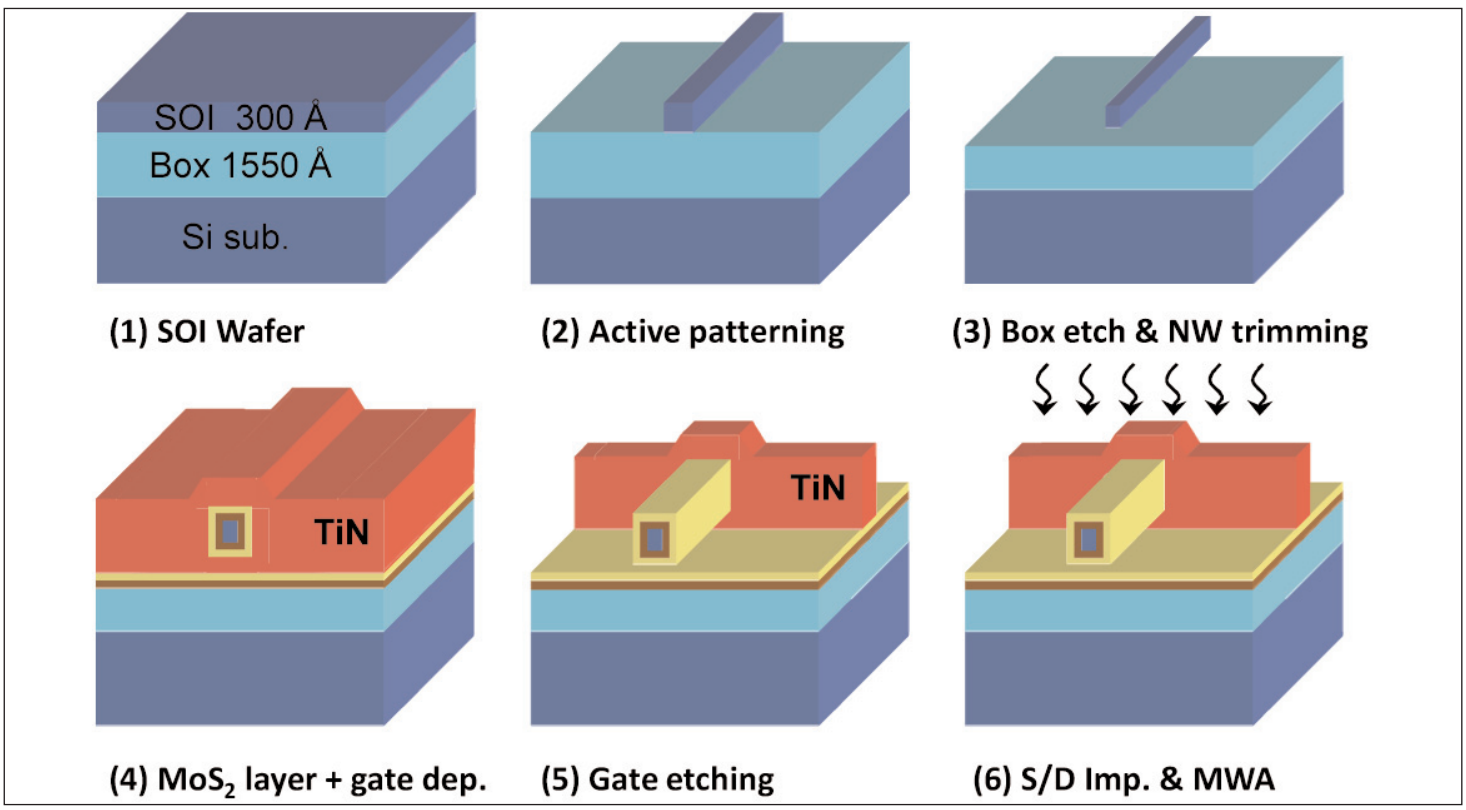

Figure 9. Schematic of nanowire FET with hybrid Si/MoS_2 channels.